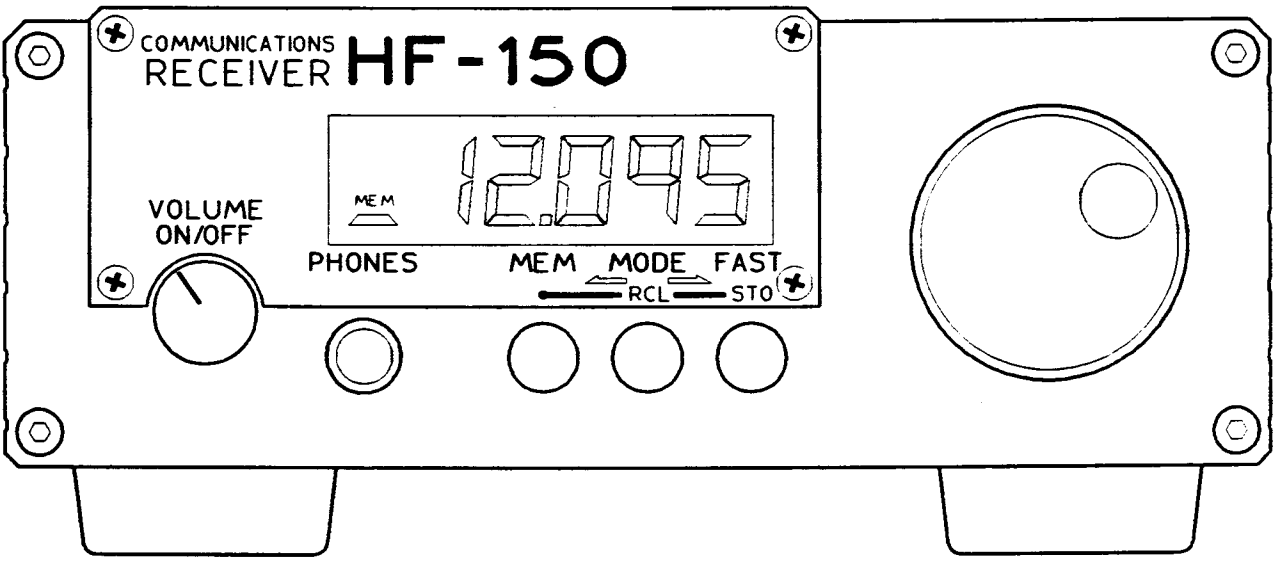
HF·150

TECHNICAL MANUAL

HF-150 General Coverage Receiver.

Technical Manual.



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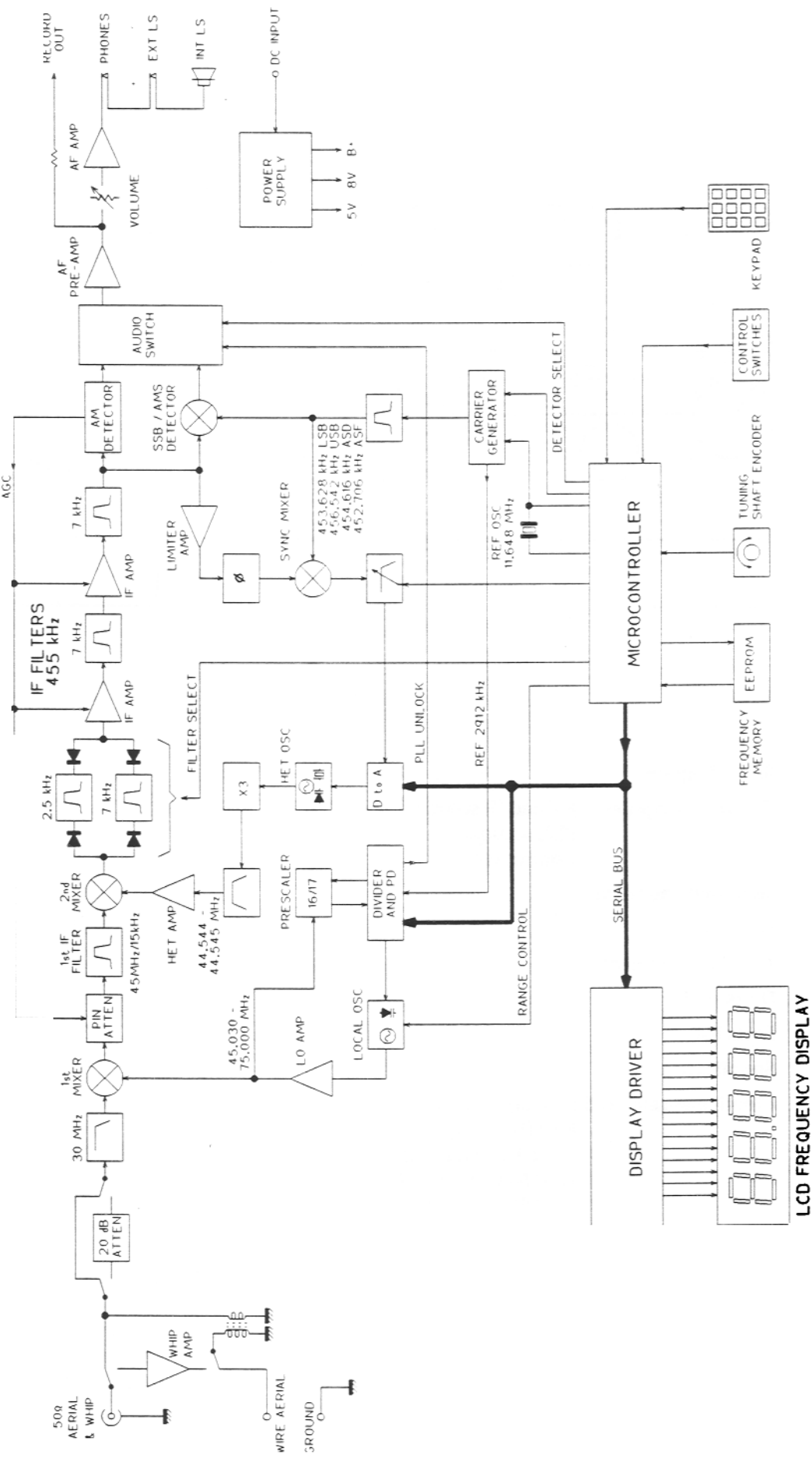

HF 150 BLOCK DIAGRAM
LCD FREQUENCY DISPLAY
50Ω AERIAL & WHIP
WIRE AERIAL
GROUND
WHIP AMP
20 dB ATTEN
30 MHz
1st MIXER
PIN ATTEN
1st IF FILTER
45MHz/15kHz
2nd MIXER
HET AMP
44.544 - 44.545 MHz
45.030 - 75.000 MHz
LO AMP
LOCAL OSC
PRESCALER
16/17
DIVIDER AND PD
RANGE CONTROL
X3
HET OSC
D to A
PLL UNLOCK
REF 2912 kHz
SERIAL BUS
DISPLAY DRIVER
IF FILTERS 455 kHz
2.5 kHz
7 kHz
FILTER SELECT
IF AMP
AGC
AM DETECTOR
SSB / AMS DETECTOR
LIMITER AMP
SYNC MIXER
453.628 kHz LSB
456.542 kHz USB
454.616 kHz ASD
452.706 kHz ASF
CARRIER GENERATOR
REF OSC 11.648 MHz
DETECTOR SELECT
AUDIO SWITCH
AF PRE-AMP
VOLUME
AF AMP
RECORD OUT
PHONES
EXT LS
INT LS
DC INPUT
POWER SUPPLY
5V 8V B+
MICROCONTROLLER
EEPROM
FREQUENCY MEMORY
TUNING SHAFT ENCODER
CONTROL SWITCHES
KEYPAD

Circuit description.

1) **RF and IF section.**

1.0 Frequency configuration.

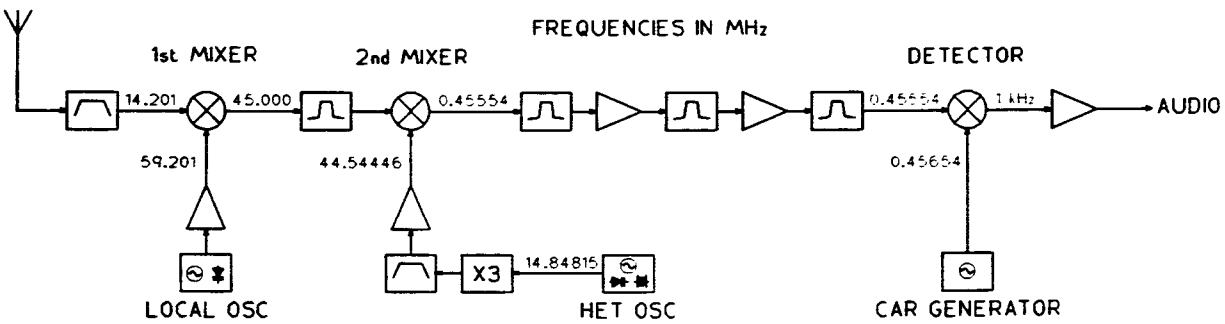
The HF-150 is a dual-conversion superheterodyne receiver, using intermediate frequencies of 45 MHz and 455 kHz in its two IF stages. R F signals are converted to 45 MHz by the local oscillator signal (LO) which is tuned from 45.030 MHz to 79.999 MHz to give 30 kHz to 30 MHz receiver coverage. The local oscillator is tuned in 1 kHz steps.

Conversion between the two IF's is by the heterodyne oscillator signal (HET) which is tuned over a 1 kHz range between 44.544 and 44.545 MHz. The frequencies of LO and HET are varied together by the microcontroller to give continuous receiver tuning.

The filters in the 2nd IF are centred on 455 kHz. This frequency corresponds to the tuned frequency in AM and AMN modes, but the IF is offset above or below 455 kHz in the sideband modes so that only the correct signals pass through the filters. The offset is provided numerically within the microcontroller program.

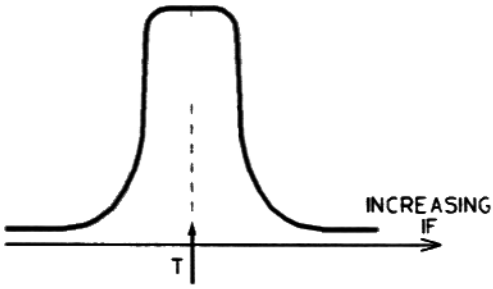
SSB mode and synchronous AM mode audio is derived by mixing the final IF with a carrier reinsertion signal (CAR). The frequency of this reflects the IF offset, ie 456.54 kHz in USB / ASU mode and 453.63 kHz in LSB / ASL mode. In ASF mode the IF is offset by 2.3 kHz towards the lower sideband to give the widest possible audio frequency response through the 7 kHz filter.

Because the local oscillator frequency is higher than the 1st IF, the RF frequency spectrum is reversed in both IF stages, so an increase in signal frequency produces a corresponding decrease in intermediate frequency.



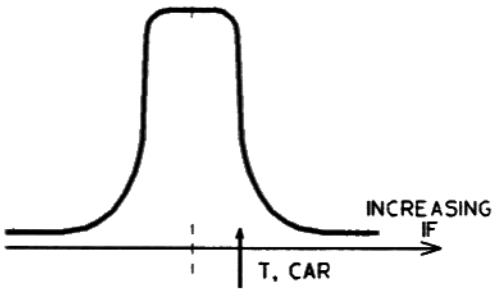
Oscillator and IF frequencies with the receiver tuned to 14.200 MHz, USB.

The following diagrams show the relationship between tuned frequency, IF filter centre frequency and carrier reinsertion frequency for each mode.



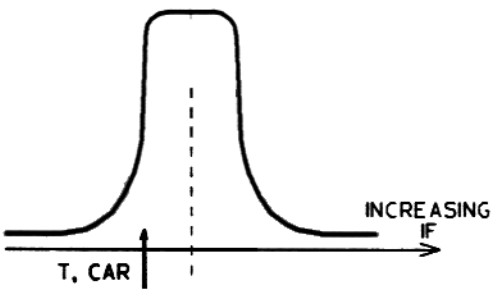
AM and AMN modes:

Tuned frequency (T) in centre of filter passband.



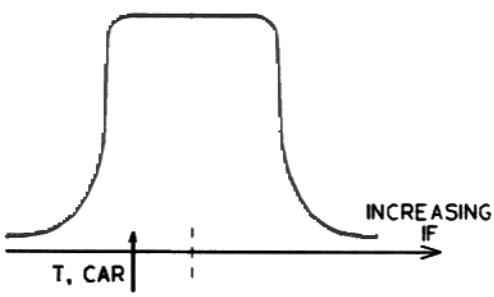
USB and ASU modes:

Tuned frequency (T) offset by -1.54 kHz.
Carrier reinsertion (C) offset by +1.54 kHz.



LSB and ASL modes:

Tuned frequency (T) offset by +1.37 kHz.
Carrier reinsertion (C) offset by -1.37 kHz.



ASF mode:

Tuned frequency (T) offset by +2.3 kHz.
Carrier reinsertion (C) offset by -2.3 kHz.

1.1 Aerial input circuits.

The aerial input switching and filtering circuits convert the three aerial inputs to a standard 50 ohm impedance and apply an elliptic 30MHz low pass filter to remove image and IF responses. The filter, comprising L9 / L10 / L11 and associated capacitors, is arranged with its first pole at 45MHz (adjusted by TC3) to provide good 1st IF rejection.

The whip aerial amplifier is Q19, a JFET arranged in common source configuration, giving a high input impedance at low frequencies and about 10dB of gain. A small amount of voltage feedback improves amplifier linearity. Transformer T2 is used for both output matching of the whip amplifier and impedance conversion at the 600 ohm wire aerial input. Aerial attenuation is provided by R65 for the wire input and R66 / R67 for the 50 ohm input.

1.2 1st mixer and 1st IF.

An SL6440 integrated circuit, transistor tree mixer Q22 is used to convert the RF signal to the first IF at 45 MHz. Transformer T3 provides a balanced signal feed to the mixer, and the balanced output is matched to the crystal filter X4 by a tuned transformer T4. In this configuration the mixer provides enough gain to remove the requirement for a separate RF amplifier stage for normal aerial inputs, and offers about 90 dB of intermodulation-free dynamic range.

AGC is fed back from the detector stage, via current control Q21, to a PIN attenuator diode D17. This controls the gain of the mixer by altering its output impedance. Mixer operating current is set by R74, and the stage is fed from the unregulated B+ supply to maximise dynamic range.

1.3 2nd mixer and 2nd IF.

The second IF section is a cascade of three filters, interspersed with two amplifier stages. There are no adjustments in this section. The IF at 455 kHz is produced by the second mixer, which is also an SL6440 IC, but it is operated at a much reduced current compared to the first mixer. The 15 kHz bandwidth of the first IF filter reduces the dynamic range requirement of the second mixer.

The second mixer output is applied directly to the filters that determine the IF bandwidth; either the wide or narrow filter is selected by the FLT line from the control system. Diode switching passes the IF signal through either the 2.5 kHz filter (X5) or the 7 kHz filter (X6).

Both of the IF amplifier stages are contained in the SL6700 detector IC, Q32. AGC control to these amplifiers is provided within the integrated circuit. A 7 kHz filter (X8) is placed between the two amplifiers and another 7 kHz filter (X7) comes after the second amplifier and before the AM and SSB detectors. Transistor Q31 increases the IF signal level to the SSB product detector and the synchronous AM detector system.

1.4 Detectors and AGC system.

The SL6700 IC contains both the AM envelope detector and the mixer used for SSB and synchronous AM, the AGC system and an impulse noise blanker. A full-wave detector provides the AM audio output and feeds an IF signal level to the AGC system. The AGC time constant is provided by C97 and C98 in all modes. Transistors Q28 and Q30 provide a fast AGC attack for SSB mode, but this is disabled by Q29 during noise impulses and when the local oscillator is tuning.

The synchronous AM lock circuit is based around the MC3357 FM IF integrated circuit. This contains limiting amplifiers and mixers used to extract the AM carrier from the IF signal and phase-compare it with the receiver's carrier injection. The phase correction voltage is buffered by Q11 and used to fine-tune the Heterodyne oscillator (and thus the receiver).

1.5 AF stages.

Audio switching between the SSB/sync and AM detectors is carried out by a CMOS switch Q18. Resistors R85 and R86 balance the levels of the two signals by controlling the gain of preamplifier Q11. Muting is applied by the controlling logic gates in Q26, which turn both detector signals off when the PLL system is unlocked or when an external mute is applied.

The preamplifier output is fed to the record out jack at a constant level, and via the volume control and high-pass filter C82 to the AF amplifier and to the loudspeaker. The final amplifier is fed from the unregulated B+ supply to maximise available audio output power.

1.6 Power supply.

Three supply rails are used in the receiver :-

5 Volts for the logic and control system, 455 kHz IF amplifiers and signal switching.

8 Volts for the 45 MHz IF stages, the PLL system and HET oscillator, and the audio preamplifier.

An unregulated supply between 9V and 15V (B+) for the first mixer and the audio amplifier.

The 8V and 5V supplies are provided by regulators Q16 and Q17 from the B+ supply. A low voltage drop regulator (LP2950 series) is used for the 8V rail to give a stable supply under battery operation when B+ may only be 9V. This regulator also provides a low-battery detection output to the control system.

If batteries are fitted to the receiver they will power the receiver when there is no plug in the DC power input jack. If the receiver is operating from an external supply, the batteries are maintained with a small trickle charge of a few mA via D15 and R55 / R56. When the receiver is switched off, the cells are reconnected as two 4.8V batteries in parallel, and the charging current increases to about 45 mA for each cell. To avoid damage, non-rechargeable cells should be removed when the set is used from an external supply. Diode D14 provides protection against a reverse-polarity supply connection, but care should be taken that the normal supply does not exceed 16V. Current consumption is 130 to 250 mA in normal use, depending on the audio output level.

2) PLL section.

2.0 Frequency configuration.

The PLL system and two other signal sources grouped in this section produce the local oscillator (LO), heterodyne (HET) and carrier (CAR) signals that are fed to the IF mixers. There is no signal interconnection between these sources, but their frequencies are controlled together in order to tune the receiver.

The following frequency relationships apply :-

Received frequency = <LO> - <HET> - 455 kHz in AM mode.

Received frequency = <LO> - <HET> - <CAR> in SSB and AM sync modes.

2.1 Carrier generator.

The carrier generator circuit is located on the control unit board and consists of a programmable digital divider followed by a filter and amplifier. The programmable divider takes its input from the 11.648 MHz reference oscillator in the microcontroller, Q1, after division to 2912 kHz by Q5. When a carrier signal is needed (in all modes except AM and AMN) divider Q4 is enabled with an appropriate division ratio to produce the required carrier frequency for the particular mode. The microcontroller uses three program lines CPA, CPB and CPC to control the division ratio.

Selected Mode	Division ratio	Program A	B	C	Divider o/p frequency	Selected harmonic	CAR frequency
LSB / ASL	199	1	1	0	14.6332 kHz	31 st	453.628 kHz
USB / ASU	236	0	0	1	12.3390 kHz	37 th	456.542 kHz
ASD	237	1	0	1	12.2869 kHz	37 th	454.616 kHz
ASF	238	0	1	1	12.2353 kHz	37 th	452.706 kHz
test	197	1	0	0	14.7817 kHz	31 st	458.234 kHz

The output from the programmable divider is a stream of short pulses, containing many harmonics of the fundamental frequency. This pulse stream is fed through a 7 kHz bandwidth ceramic filter which selects one harmonic near to 455 kHz. This is then amplified by Q3 and fed to the product detector.

2.2 Heterodyne oscillator.

The heterodyne oscillator, Q14 / X3, is a fundamental mode crystal oscillator running at about 14.848 MHz. The diode D8 in the drain of FET Q14 is operated in its non-linear region and produces strong harmonics of the fundamental frequency. The third harmonic at 44.545 MHz is selected by tank circuit C40 and L5, amplified by Q24, and fed to the second mixer.

The oscillator frequency is adjusted by TC2 and also by the bias voltage on varicap diode D4. A change of about 0.6V in bias will move the oscillator frequency by 330 Hz, resulting in a 1 kHz change of HET frequency. The bias voltage is derived from a section of the Q11 op-amp which acts as a current-to-voltage converter driven through an R - 2R - 4R ... resistor chain (R38 to R45) from a 7-bit control register, Q10. The HET frequency can be controlled in 128 steps across its 1 kHz range, each step being nominally 7.8 Hz. In synchronous AM mode an additional control voltage is fed in from the sync IF phase detector to fine-tune the receiver and lock it to the incoming signal.

Variable resistor VR1 adjusts the span of the HET oscillator tuning. Component values in the current-to-voltage converter are chosen so that the setting of VR1 has little effect at the highest bias voltage (corresponding to maximum HET frequency and minimum tuned frequency), allowing VR1 and TC2 to be adjusted independently.

2.3 Local oscillator.

The local oscillator, Q13, is a wide range VCO tuning from 45 MHz to 75 MHz. A JFET is used as the gain element to provide a low-noise signal which is buffered by Q15 then fed to the first mixer and the PLL system divider. The oscillator is tuned by varicap diode D3 controlled from the PLL system. Two frequency ranges are available depending on the control voltage applied to PIN diode D5. which selects the required inductance value of oscillator coil T1. The high / low change point for the oscillator corresponds to a received frequency of 11.576 MHz

2.4 PLL system.

The PLL system controls the frequency of the local oscillator using a crystal-derived reference of 2912 kHz from the control system. All of the functional blocks of the PLL system are contained in Q7 but a prescaler, Q8, is also required to reduce the local oscillator frequency so that Q7 can operate correctly. Q8 is a dual-modulus prescaler, and can divide by 16 or 17 under the control of Q7 in a pulse-swallowing counter. This counter is arranged as a programmable divider, where the division ratio can be controlled by the receiver's microcontroller.

Both the LO signal and the reference are divided down to 1 kHz and applied to phase detector circuits in Q7. When the phase error is large, a linear digital phase detector can correct the error quickly. As the phase error becomes small, the digital detector becomes inactive and an analogue sample-and-hold detector is used instead. This can only correct small phase errors, but offers much better residual noise performance than the digital detector. When the digital detector operates, the out-of-lock output from Q7 goes high, muting the receiver audio.

Both phase detector outputs go to an active integrating loop filter formed by op-amp Q11. The output from this is further filtered by R19 / C17 and then controls varicap diode D3 in the oscillator circuit. To increase the available voltage swing on the tuning diode, its cathode is held at 2 volts below ground. The negative potential is derived from a charge pump C27 / D6 / D7 / C28, driven by an output at 56 kHz from the PLL IC, Q7.

3) Control section.

3.0 Microcontroller and control program.

At the centre of the control system is the microcontroller Q1. This integrated circuit contains all of the elements of a microprocessor system - program memory (ROM), data memory (RAM), a central processing unit and input and output ports. With the exception of the clock oscillator all lines into and out of the microcontroller are in a static condition unless the receiver's controls are operated, so the signals radiated by the control system are kept at a very low level.

The microcontroller chip contains a control program specific to the HF-150 receiver. This program provides an interface between the operator and the receiver's tuning and filter selection systems, and also provides additional features such as frequency memories. The program accepts commands from the tuning encoder, the function buttons and the remote keypad, and in turn controls the display, the IF filters, the PLL system and the heterodyne oscillator.

When the control system is in an idle condition, with no controls being operated, the control program remains in a monitoring loop looking for any changes in the controls. If any control is moved, the program detects this and modifies its internal status to suit. This may involve just changing internal memory values, or it may require data to be sent to the display or the receiver control registers. There are three subprograms in the monitoring loop, dealing with the tuning knob, the function buttons and the external keypad.

As an example of the operations performed by the control program, consider the action of the program in response to rotation of the tuning knob.

Tuning encoder rotation is detected :-

Establish direction of rotation (up/down).

Establish speed of rotation (fast/slow).

Check mode selected and look-up tuning rate from internal table.

Increase or decrease stored frequency value by tuning rate value.

Check the new tuning value against the operating frequency limits and inhibit tuning if these are exceeded.

If the kHz digits have changed, convert the frequency value into 7-segment digits and send this data to the display.

Select the appropriate local oscillator frequency range.

Convert the frequency value into binary form suitable for programming the PLL synthesiser and add an offset value depending on the mode selected.

Send the new frequency information to the heterodyne oscillator and, if they require reprogramming, to the PLL control registers.

Store the new frequency value in external non-volatile memory.

Check the tuning encoder for further rotation, and either repeat this sequence or return to the monitoring loop.

All tuning of the receiver is done in terms of fine-tune steps. Each 1 kHz of tuning range is divided into 128 steps, so each step is approximately 8 Hz. One complete rotation of the tuning encoder generates 200 pulses, and each of these pulses will change the frequency by a preset number of steps. The number depends on the tuning rate and the mode selected according to the following table :-

Receiver Mode	Tuning increments (steps of 7.8 Hz)	
	Slow tuning rate	Fast tuning rate
LSB, USB	1	8
AM, AMN	7	50
ASD, ASF	1	50 *
ASl, ASU	0.5	50 *

* Synchronous AM modes switch to AM when fast tuning is detected, and return to the original mode after about 2 seconds.

The fast or slow tuning rates are selected according to the rate at which pulses come from the tuning encoder. Note that in practice the fast tuning rate will not be as fast as indicated in the table because some pulses from the encoder will be missed by the control program (when it is involved in other tuning operations), therefore rapid rotation of the tuning knob usually results in a mixture of fast and slow tuning rates.

As each new kHz frequency is tuned the control program establishes which local oscillator frequency range to select. The same part of the program also checks the frequency range limits, which are normally 30 kHz minimum and 29999 kHz maximum. The limits may be restricted further to frequencies above 150 kHz by insertion of an optional diode on the control unit, which can be sensed by the control program and modifies its operation. Frequencies outside the limits, whether derived from the memories or entered from the external keypad, are converted to the nearest limit frequency.

3.1 Controls.

The front panel controls connect to the microcontroller through input ports. The three function buttons each pull an input line down to ground when pressed; there is a pull-up resistor to 5V inside the microcontroller chip. Tuning knob rotation is detected by a mechanical shaft encoder, which generates two streams of pulses which differ in phase. The controller is able to establish the speed and direction of tuning from these two signals after pulse shaping and glitch removal by R / C filtering circuits.

3.2 Frequency memory.

Frequencies stored in the receiver's memories are not held within the microcontroller, but are stored in an EEPROM chip Q2, a device which will retain information without need of a power supply. The tuned VFO frequency must also be stored in this memory so that the receiver can resume operation on its previous frequency at switch-on. Due to write-cycle limitations with the EEPROM this frequency cannot be saved every time it is changed, but instead a "crash save" strategy is used when the microcontroller detects a power failure - power supply regulator Q17 detects low supply voltage, and the current frequency and mode are saved within 10 ms.

Inside the receiver, frequencies are stored in the form of separate decimal digits for the kHz part (5 digits) and a 7-bit binary value for the fine tune part (fractions of kHz). The external frequency memory chip is 32-bits wide by 64 locations; each frequency uses one location - 20 bits for the kHz digits, 8 bits for the fine tune value and 4 bits for the mode. There is room in the memory for 64 frequency entries, but only 60 are used for the memories and one for the VFO frequency. Q2 is not attached to the microprocessor bus, but is controlled via a 4-line serial interface - clock (CLK) and strobe (CS) lines from the microcontroller and data in (SD) and out (DO).

3.3 Display.

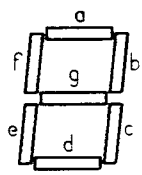
The liquid crystal frequency and function display is driven from a dedicated controller Q6. The LCD segments turn on when a voltage exists between the segment line and the backplane or common. It is important that there is no residual current flow through an LCD, so the segments are driven with a low frequency AC supply produced inside Q6 by oscillator R12 / C9. The backplane connection is fed with a square wave at about 60 Hz, and blank segments are fed with an identical signal. Lit segments are fed with a signal in antiphase to the backplane.

Segment data is transferred from the microcontroller to the display driver by a two-line serial bus; DSD and CLK. Data transfer commences when the data line goes high and the clock line pulses high, then the state value of each segment is placed on the data line and the clock line pulsed high again for each segment. Transfer is complete when 35 bits of data have been sent, and then the display will be changed to the new configuration. Further clock pulses will be ignored until the data line goes high again.

Display driver serial data format :-

Bit 0 (start)	always high (1)		Bit 18	digit 3	seg g
Bit 1	digit 6	seg c	Bit 19		seg f
Bit 2		seg d	Bit 20		seg a
Bit 3		seg e	Bit 21		seg b
Bit 4	digit 5	seg c	Bit 22	digit 4	seg g
Bit 5		seg d	Bit 23		seg f
Bit 6		seg e	Bit 24		seg a
Bit 7	digit 4	seg c	Bit 25		seg b
Bit 8		seg d	Bit 26	digit 5	seg g
Bit 9		seg e	Bit 27		seg f
Bit 10	digit 3	seg c	Bit 28		seg a
Bit 11		seg d	Bit 29		seg b
Bit 12		seg e	Bit 30	digit 6	seg g
Bit 13	decimal point		Bit 31		seg f
Bit 14	digit 2	seg c	Bit 32		seg a
Bit 15		seg b	Bit 33		seg b
Bit 16		seg a,d,e,g	Bit 34	always low (0)	
Bit 17	memory flag		Bit 35	always low (0)	

Digit 2 = 10's MHz (Only blank, 1 or 2)
Digit 3 = units MHz
Digit 4 = 100's kHz
Digit 5 = 10's kHz
Digit 6 = units kHz



3.4 Receiver interface.

The frequency control functions within the receiver are controlled via a three line serial bus from the microcontroller, which sends data to registers located on the main receiver circuit board. The three lines (CLK, SD and STRB) are supplemented by direct control lines for detector selection (DET and (SYN) and filter bandwidth (FLT).

The serial data is converted into steady-state signals for tuning by two cascaded shift registers, Q9 and Q10, each 8-bit registers. Because not all of the control lines need to change when the PLL chip registers are loaded, the shift register can be split into a shorter 8-bit section. To set the receiver frequency, a data stream of the appropriate length is sent from the microcontroller, each data bit separated by a clock pulse (the CLK line goes momentarily high). The end of the data stream is marked

by the STRB line pulsing high. Note that the CLK signal is shared between the display driver, the EEPROM and the receiver control, so there will be spurious data and clock signals fed into the registers; only the data stream before a STRB pulse has any effect on the receiver.

The format of receiver frequency data is shown below :-

Format 1: 8-bit data, PLL register load.

Bit 0 (start)	PLL register data bit 3 (msb)
bit 1	PLL register data bit 2
bit 2	PLL register data bit 1
bit 3	PLL register data bit 0
bit 4	PLL register address bit 0
bit 5	PLL register address bit 1
bit 6	PLL register address bit 2
bit 7	ZERO to select 8-bit shift register length

Format 2: 16-bit data, HET oscillator tune.

Bit 0 (start)	Local oscillator range select (0 = HF, 1 = LF)
bit 1	HET tune data bit 6 (msb)
bit 2	HET tune data bit 5
bit 3	HET tune data bit 4
bit 4	HET tune data bit 3
bit 5	HET tune data bit 2
bit 6	HET tune data bit 1
bit 7	HET tune data bit 0 (lsb)
bit 8	ZERO
bit 9	ZERO Null command to PLL chip
bit 10	ZERO (address = 0)
bit 11	ZERO (data = 0)
bit 12	ZERO
bit 13	ZERO
bit 14	ZERO
bit 15	ONE to select 16-bit shift register length

The PLL synthesiser chip Q7 is programmed on a register by register basis, each one of eight registers selected by the three address lines. To change the PLL frequency, seven of the registers need reprogramming, the remaining register is programmed only when the receiver is first switched on. The programmable divider in Q7 is set with a 17-bit binary number, which is the PLL frequency in kHz.

PLL chip register contents are as follows

Register	Address bits			Data bits				
	A2	A1	A0	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	Used as Null command
1	0	0	1	N3	N2	N1	N0	
2	0	1	0	1	0	0	0	Loaded at switch-on
3	0	1	1	N7	N6	N5	N4	
4	1	0	0	0	N10	N9	N8	
5	1	0	1	N14	N13	N12	N11	
6	1	1	0	0	0	N16	N15	
7	1	1	1	1	1	1	1	End programming sequence

The three direct control lines function as follows :-

Line	Function	States
DET	Detector select	low = envelope detector
		high = product detector
SYN	Synchronous enable	high = enable
FLT	IF filter select	low = 2.5 kHz
		high = 7 kHz

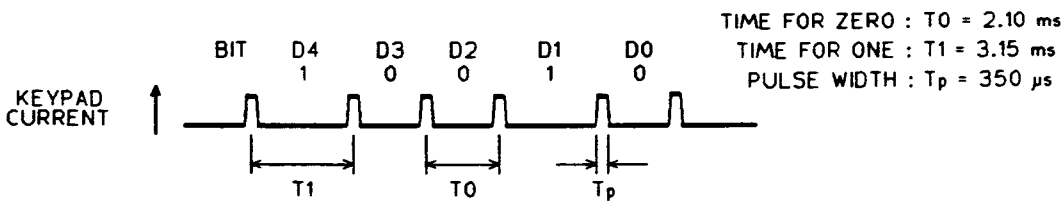
3.5 External keypad.

The remote keypad, KPAD-1, uses a two-wire serial link to communicate with the receiver. Key depressions are converted into an asynchronous PPM (pulse position modulation) data stream by integrated circuit Q1 - each key is uniquely represented by a 5-bit word which is sent repetitively whilst the key is held down. Power for the keypad unit is also sent down the two wires, and data is transmitted by current modulation of this supply. Transistor Q4 is switched by the data output of Q1 to achieve this.

The keypad unit current passes through R59 and R60 on the receiver's main unit board, and with Q20 this serves to recover the PPM data. Q20 is normally turned off, but when the keypad is operated, charge pump C50 / D18 provides bias to switch the transistor on except for a short period during each data pulse. The PPM data is presented to the microcontroller on the KEY line - data stream decoding is done by software within the microcontroller. When a key on the keypad is released, Q20 turns off after a short delay.

Each key code is transmitted as a series of six current pulses, with the five time intervals between the pulses changed according to the data. The time between pulses may be either 3.15ms, representing a ONE, or 2.1ms, representing a ZERO. These times are in the ratio 3:2, with the pulse width being about one sixth of the ZERO time, ie 350us. The 5-bit key codes are shown in the table below - they are transmitted continuously whilst any key is pressed, with a gap of about twice the ONE time between each code word. Additional codes, not produced by the keypad, can be sent to the receiver to implement remote control functions. These codes are used by the RS232 interface, IF-150.

An example of code is given for the key **6** (code = 1 0 0 1 0) :-



Key	Data code D4	D3	D2	D1	D0	
No key pressed	No data pulses					
0	1	0	1	0	0	
1	1	1	0	1	1	
2	1	0	1	1	1	
3	1	0	0	1	1	
4	1	1	0	1	0	
5	1	0	1	1	0	
6	1	0	0	1	0	
7	1	1	0	0	1	
8	1	0	1	0	1	
9	1	0	0	0	1	
Cancel (*)	1	1	0	0	0	
Enter (#)	1	0	0	0	0	
Store into mem	1	1	1	1	0	and 6-bit memory number
Set fine tune	1	1	1	1	1	and 8-bit fine tune value
Select LSB mode	0	0	1	0	0	
Select USB mode	0	0	1	0	1	
Select AMN mode	0	0	1	1	0	
Select AM mode	0	0	1	1	1	
Select ASD mode	0	1	0	0	0	
Select ASF mode	0	1	0	0	1	
Select ASL mode	0	1	0	1	0	
Select ASU mode	0	1	0	1	1	

3.6 Test routines.

A small part of the control program is devoted to test and alignment routines. These check for the correct operation of parts of the control system and provide signals and conditions convenient for testing and aligning the receiver. The control system tests are not exhaustive, and the fact that the test routines do not report an error should not be used as verification of a faultless unit, but many errors can be detected, and often the type of fault reported is a useful guide to repair.

In test mode the three buttons on the front panel serve to control the program. The receiver is set into test mode by depressing the **MEM** button as it is switched on, and the message **TEST** should appear on the display. This message will remain on the display provided that no faults are found, if a fault condition is detected the display changes to show the **FLT** message. To clear a fault indication or to exit from test mode the receiver must be switched off.

For instructions on how to use the test routines for checking and alignment, please refer to the **Test and Alignment** section of this manual. Here, the testing procedures used by the program are outlined.

When the receiver is switched on without the **MEM** button held a brief check is performed on the program memory and microprocessor registers. A failure in this test will result in a fault indication immediately and the receiver will not operate. The remaining tests are initiated by pressing one of the front panel buttons. Most tests will operate continuously whilst a button is held, allowing serial data lines to be monitored with test equipment.

Enters TEST mode from switch-on, and sends the test message to the display. Programmes and tests the frequency memory EEPROM chip. Note that any frequencies saved in memories 54 to 60 will be lost when test mode is entered. A fault indication will result if data corruption is detected. The frequencies stored in the upper memories can be later used to test local oscillator alignment (see below).

MODE Programmes the receiver control registers for alignment phase 1 (see below).

Programmes the receiver control registers for alignment phase 2 (see below).

Alignment frequencies entered in memory during test mode :-

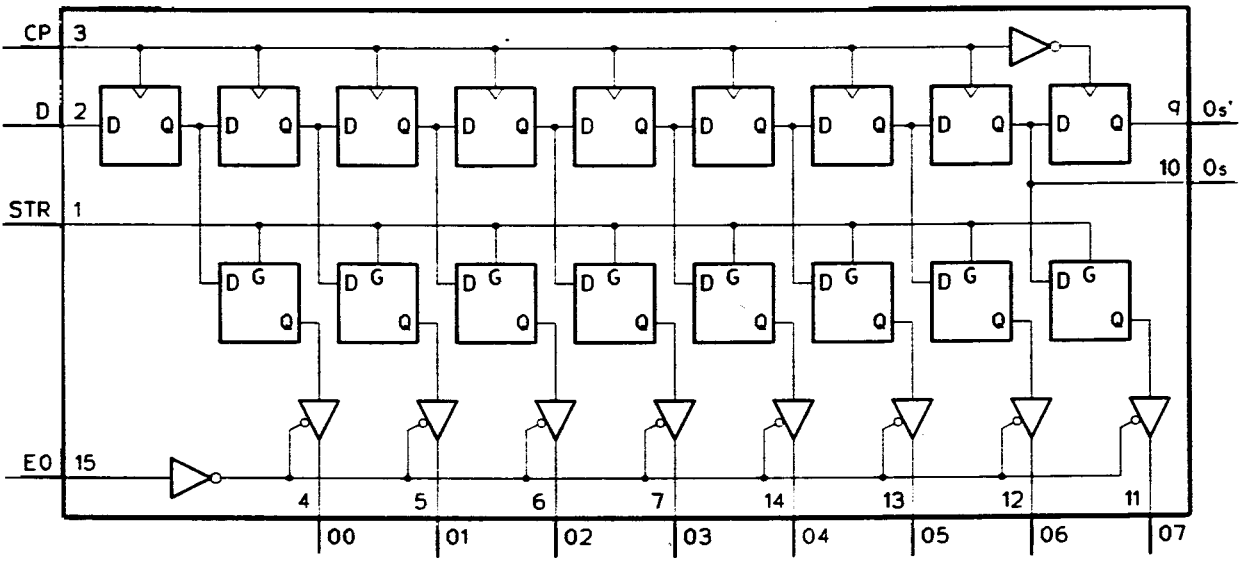
Memory number	Frequency	Purpose
54	USB	
55	AM	Local osc range 1 LF check
56	AM	Sensitivity check
57	AM	Local osc range 1 HF check
58	Am	Local osc range 2 LF check
59	AM	Local osc range 2 HF check
60	USB	

Receiver state setup during alignments :-

Phase 1	IF filter	Wide, 7 kHz
	Detector select	Product detector, sync off
	Car generator frequency	458.234 kHz
	Local osc frequency	45.000000 MHz
	Het osc data	0000000
	Het osc frequency	44.545000 MHz
Phase 2	As above, except	
	Local osc frequency	44.999000 MHz
	Het osc data	1111111
	Het osc frequency	44.544008 MHz

Semiconductor data.

74HC4094T Shift and store bus register, Q9 and Q10.



The 4094 consists of an 8-bit shift register, transparent latch and tri-state output buffer. The shift register is loaded serially on the positive edge of each CP pulse. Serial data from the last stage of the register is presented at the Os output, and, delayed until the negative edge of CP, on the Os' output. (Os' is used for cascading several registers).

Parallel data from the shift register is transferred to the latch when the STR line is high, and retained while STR is low, so the outputs are unaffected by shift register activity. The outputs are buffered with tri-state devices, but in the HF-150 these are permanently enabled.

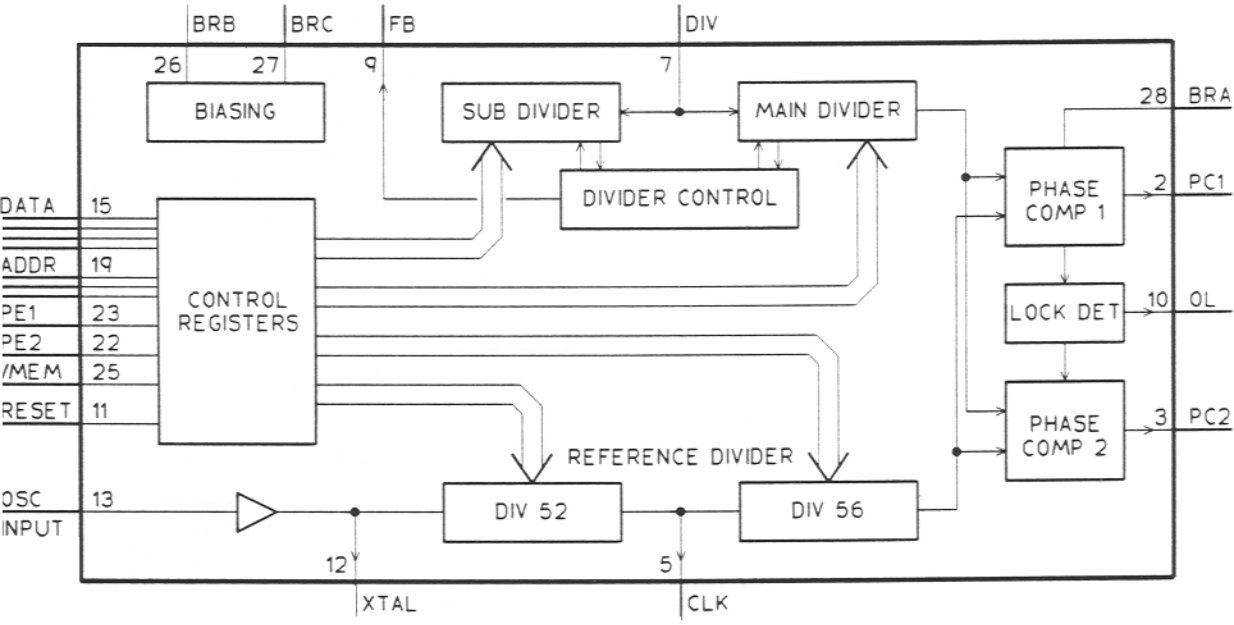
Q9 pin functions.

Pin	Name	I/O	State	Function	Pin	Name	I/O	State	Function
1	STR	In	H	Always high	9	Os	Out	L / H	No connection
2	D	In	L / H	SD, changes during tuning	10	Os'	Out	L / H	Serial data, changes during tuning
3	CP	In	L [H]	CLK, pulses high during tuning	11	O7	Out	H [L]	PLL D3, pulses high during tuning
4	O0	Out	L [H]	Reg load, pulses high during tune	12	O6	Out	L [H]	PLL D2, pulses high during tuning
5	O1	Out	L [H]	PLL A2, pulses high during tuning	13	O5	Out	L [H]	PLL D1, pulses high during tuning
	O2	Out	L [H]	PLL A1, pulses high during tuning	14	O4	Out	L [H]	PLL D0, pulses high during tuning
	O3	Out	L [H]	PLL A0, pulses high during tuning	15	EO	In	H	Always high
	Vss		L	Ground	16	Vdd		H	5V supply

Q10 pin functions.

Pin	Name	I/O	State	Function	Pin	Name	I/O	State	Function
	STR	In	L [H]	Pulses high at end of tune	9	Os	Out	L / H	No connection
2	D	In	L / H	Serial data, changes during tune	10	Os'	Out	L / H	No connection
3	CP	In	L [H]	CLK, pulses high during tuning	11	O7	Out	L / H	LO range, high=LF / low=HF
4	O0	Out	L / H	HET0, Het osc tune bit 0	12	O6	Out	L / H	HET6, Het osc tune bit 6
5	O1	Out	L / H	HET1, Het osc tune bit 1	13	O5	Out	L / H	HET5, Het osc tune bit 5
6	O2	Out	L / H	HET2, Het osc tune bit 2	14	O4	Out	L / H	HET4, Het osc tune bit 4
7	O3	Out	L / H	HET3, Het osc tune bit 3	15	EO	In	H	Always high
8	Vss		L	Ground	16	Vdd		H	5V supply

TDD1742T .PLL frequency synthesiser, Q7.



The TDD1742D contains two programmable dividers, two phase comparators and associated logic and control circuits. The reference divider is permanently programmed to divide by 2912 in the HF-150, with an intermediate tap after division by 52 giving a 56 kHz CLK signal. The main local osc divider is configured as a 13-bit binary counter, with a 4-bit sub-counter controlling the dual-modulus prescaler Q8 via the FB output.

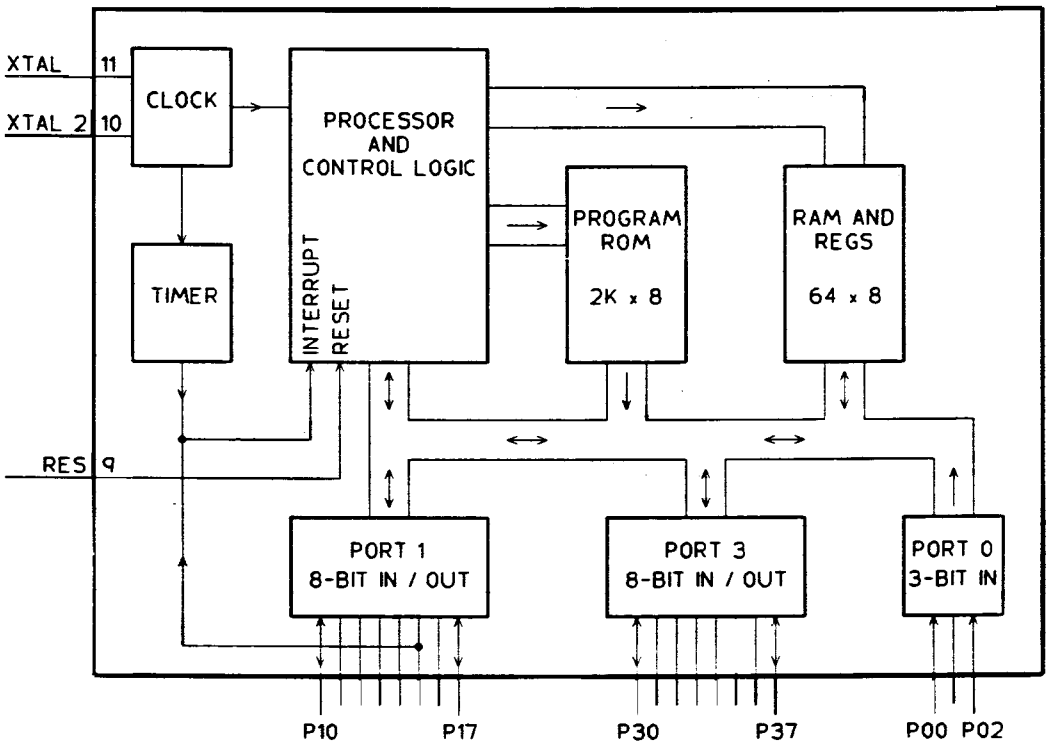
Phase comparator one is an analogue phase detector, consisting of a ramp generator and a sample-and-hold amplifier. Whilst the sampling point is within the linear region of the ramp, only this phase detector operates, but when its linear range is exceeded digital phase comparator two is enabled, and the OL (out of lock) output goes high.

The functions of Q7 are controlled by 8 internal 4-bit registers. These are loaded from the receiver's microcontroller through a 4-bit DATA bus, with register selection on the 3-bit ADDR bus. Input lines PE1, PE2 and /MEM select and control this mode of operation.

Q29 pin functions.

Pin	Name	I/O	State	Function	Pin	Name	I/O	State	Function
	Vdd3		8V	8V Supply	15	DB3	In	L [H]	PLL D3, pulses high during tuning
2	PC1	Out	4.4V	Phase comparator 1 output	16	DB2	In	L [H]	PLL D2, pulses high during tuning
3	PC2	Out	4.4V	Phase comparator 2 output	17	DB1	In	L [H]	PLL D1, pulses high during tuning
4				No connection	18	DB0	In	L [H]	PLL D0, pulses high during tuning
5	CLK	Out	SIG	56 kHz CLOCK output, 8Vp-p	19	AD0	In	L [H]	PLL A0, pulses high during tuning
6	Vss		L	Ground	20	AD1	In	L [H]	PLL A1, pulses high during tuning
7	DIV	In	SIG	LO in, 3-5 MHz, 1Vp-p on 3.5V	21	AD2	In	L [H]	PLL A2, pulses high during tuning
8	Vdd2		H	5V Supply	22	PE2	In	L	Always low
9	FB	Out	SIG	Psc control, narrow low pulses	23	PE1	In	L [H]	STRB, Pulses high during tuning
10	OL	Out	L	Out - of - lock output	24	MOD			No connection
11	RESET	In	L	Reset, pulses high at switch-on	25	/MEM	In	L	Always low
12	XTAL	Out	SIG	2912 kHz ref signal, no connection	26	BRB			No connection
13	OSC	In		2912 kHz ref input, 1.5Vp-p on 4V	27	BRC	In	4.6V	Bias current
14	Vdd1		8V	8V Supply	28	BRA	In	6.0V	Bias current

S83C751 Microcontroller, Q1. (S87C751 also used)



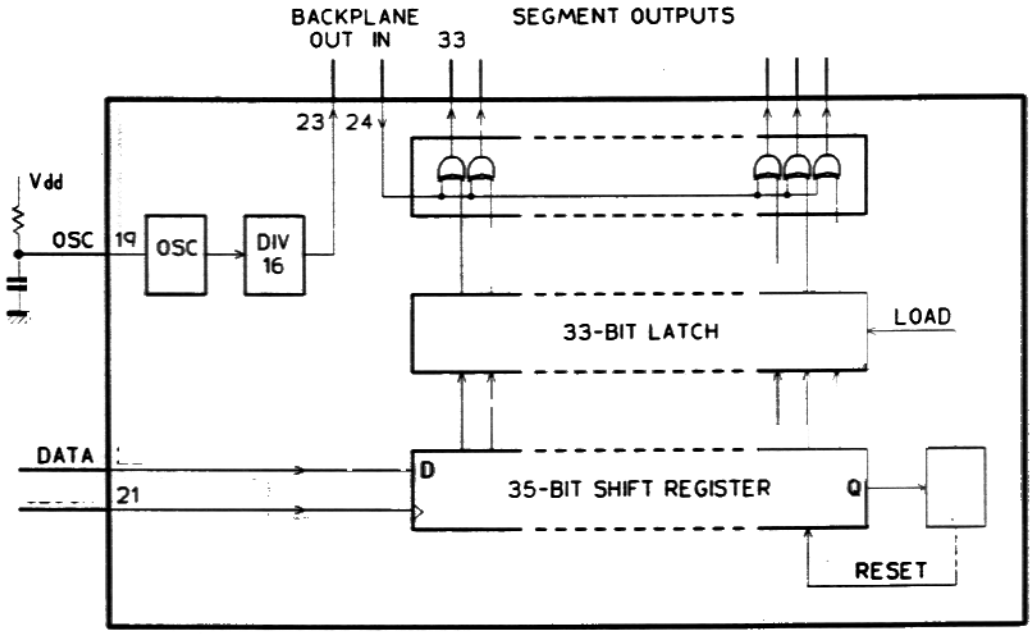
The S83C751 contains all of the parts of the microprocessor control system within the HF-150. All input and output is done via two 8-bit ports and a 3-bit port, and no microprocessor bus signals come out of the chip. The ports can be configured for either input or output; input ports other than P0 have internal pull-up resistors to Vcc.

The on-chip clock oscillator is used with an 11.648 MHz crystal as the receiver's main reference oscillator.

Q205 pin functions.

Pin	Name	I/O	State	Function	Pin	Name	I/O	State	Function
1	P3.4	Out	L [H]	STRB, receiver tune strobe	13	P1.0	Out	L / H	CPA, Carrier gen program
2	P3.3	Out	L [H]	CS, EEPROM chip select	14	P1.1	Out	L / H	CPB, Carrier gen program
3	P3.2	Out	L [H]	DSD, display driver data	15	P1.2	Out	L / H	CPC, Carrier gen program
4	P3.1	Out	L [H]	CLK, serial bus clock	16	P1.3	In	H [L]	KEY, keypad data
5	P3.0	Out	L / H	SD, serial bus data	17	P1.4	Out	L / H	DET, detector select
6	P0.2	In	L / H	DO, EEPROM data output	18	INT0	In	H [L]	PWR, power fail interrupt
7	P0.1	In	L / H	Tuning encoder phase A	19	P1.6	Out	L / H	SYN, sync detector enable
8	P0.0	In	L / H	Tuning encoder phase B	20	P1.7	Out	L / H	FLT, IF filter select
9	RES	In	L [H]	RESET, high at switch-on	21	P3.7	In	H [L]	FAST button
10	XTL2	Out	SIG	Crystal osc output	22	P3.6	In	H [L]	MODE button
11	XTL1	In	SIG	Crystal osc input	23	P3.5	In	H [L]	MEM button
12	Vss		L	Ground	24	Vcc		H	5V Supply

MM5453N Liquid crystal display driver, Q6.



LCD driver MM5453N contains a 35-bit shift register, 33-bit data latch, LCD driver buffers and a backplane signal oscillator. The data latches are loaded when a ONE bit is sent through the shift register. After the latches are loaded the shift register is also cleared, so new data has to pass through the entire length of the register before the latches are reloaded.

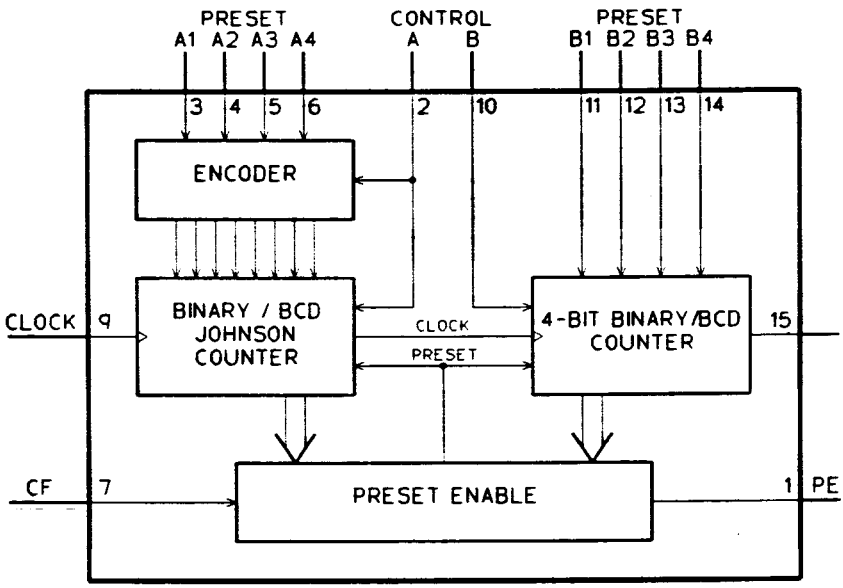
The on-chip oscillator feeds a divide by 16 counter which produces the LCD backplane signal with a 50 : 50 mark space ratio at about 60 Hz. The output drivers for each segment produce the same signal in either true or inverted form. All LCD signals swing between Ground and Vdd at 5V.

MC14569BCP Programmable divider, Q4.

The MC14569 contains two 4-bit BCD / binary down-counters that are preset from eight external inputs when the count reaches zero. In the HF-150 the chip is configured to work as a single 8-bit programmable divider. Each time the counter is preset, a pulse one clock cycle wide is produced on the PE output, this signal therefore contains many high-order harmonics of the divider output frequency. The counter is disabled when the receiver is in AM or AMN modes.

Q4 pin functions.

Pin	Name	I/O	State	Function	Pin	Name	I/O	State	Function
1	PE	Out	SIG	Counter output (see section 2.1)	9	Clock	In	SIG	2.912 MHz clock
2	CtrlA	In	L	Always low	10	CtrlB	In	L	Always low
3	PR0	In	L/H	Program CPA	11	PR4	In	L	Always low
4	PR1	In	L/H	Program CPB	12	PR5	In	L/H	Program CPC
5	PR2	In	H	Always high	13	PR6	In	H	Always high
6	PR3	In	L/H	Program CPC	14	PR7	In	H	Always high
7	CF	In	H	Enable, Low for AM mode	15	Q	Out	SIG	No connection
8	Vss		L	Ground	16	Vdd		H	5V supply

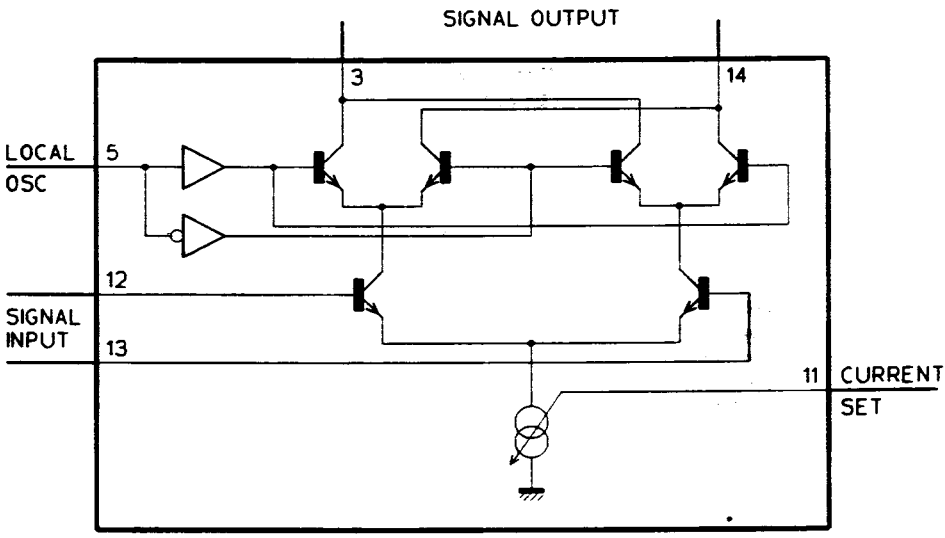


SL6440CDP High level mixer, Q22 and Q23.

The SL6440 integrated circuit, double-balanced mixer combines good strong signal performance and low noise. The mixer has balanced inputs and outputs, but either may be used unbalanced; in the HF-150 two configurations are found. Q22, the first mixer, uses balanced inputs and outputs to obtain maximum gain and lowest noise and distortion. The second mixer uses the chip with single, unbalanced input and output lines.

The mixer performance can be adjusted by an external current source into the IP pin, and the best balance of noise, intermodulation and supply current drain can be set. An amplifier for the local oscillator signal is included on the mixer chip.

Pins 1, 2, 7, 8, 9, 10, 15 and 16 are used for thermal bonding only, and are not connected within the mixer IC. In the HF-150 they are bonded to the PCB ground plane.



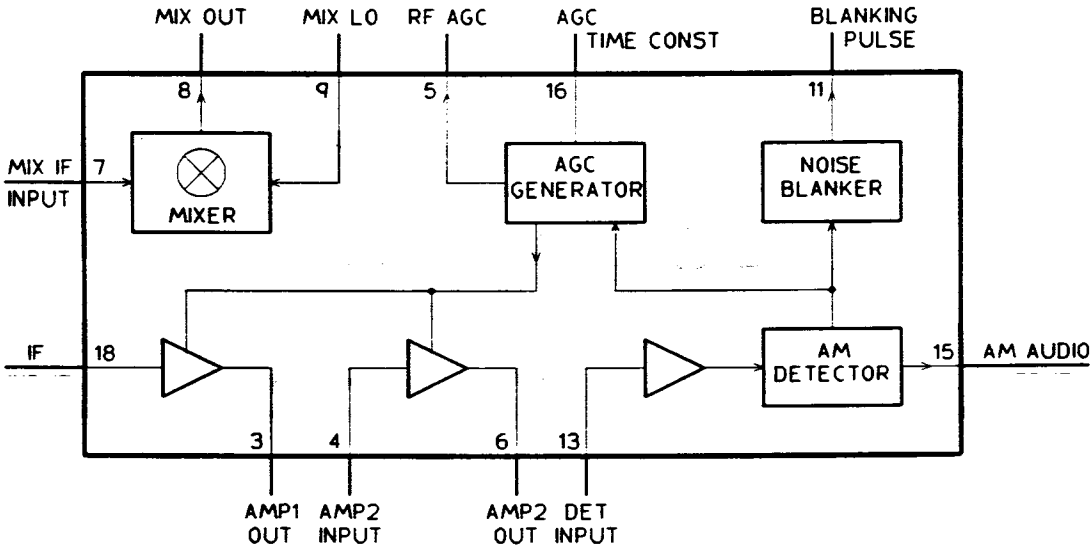
Q22 pin functions.

Pin	Name	DC Voltage	Signal	Function
3	Output A	10.9V	Some LO (<200 mV)	45 MHz IF output
4	Vcc	7.6V	None	Mixer supply
5	LO in	2.0V	LO 2Vp-p	45 to 75 MHz local oscillator input
6	0V	0V	None	Ground connection
11	IP	2.8V	None	Current program input
12	Input B	5.1V	Slight LO (<100 mV)	RF signal input
13	Input A	5.1V	Slight LO (<100 mV)	RF signal input
14	Output B	10.9V	Some LO (<200 mV)	45 MHz IF output

Q23 pin functions.

Pin	Name	DC Voltage	Signal	Function
3	Output A	7.1V	Some HET (<100 mV)	Unused output
4	Vcc	5.8V	None	Mixer supply
5	LO in	2.1V	HET 800mVp-p	44.545 MHz heterodyne oscillator input
6	0V	0V	None	Ground connection
11	IP	1.7V	None	Current program input
12	Input B	3.8V	None	Unused input
13	Input A	3.8V	Slight HET (<20 mV)	45 MHz IF input
14	Output B	7.1V	Some HET (<100 mV)	455 kHz IF output

SL6700C IF amplifier and AM detector, Q32.



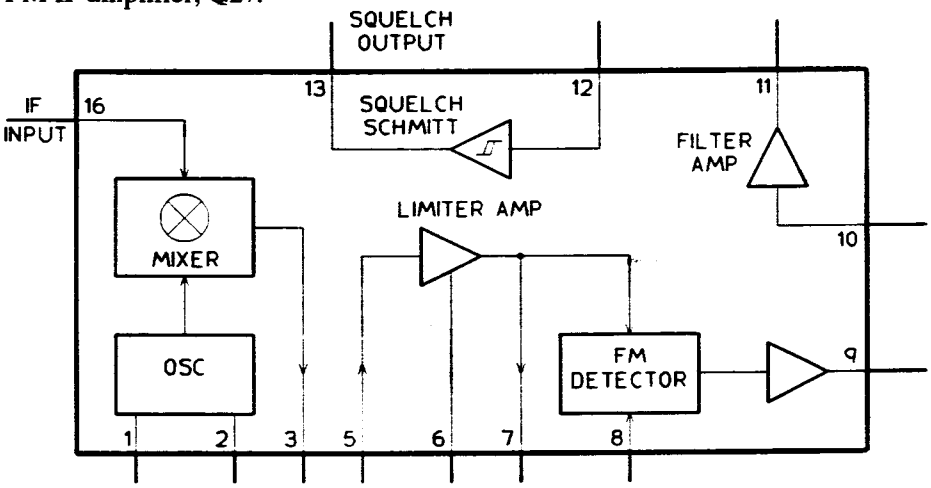
The two IF amplifiers in this chip are both broad-band devices offering about 25dB of gain with AGC control. AGC is produced internally from the AM detector, and these two amplifiers give a combined AGC range of 80dB. A level comparator on the AGC line produces a delayed AGC output for RF stages on pin 5. The value of the resistor between pins 1 and 2 sets the delay threshold.

A full-wave detection system is employed, giving excellent linearity and producing a DC carrier level output to derive AGC. This level can also trigger the noise-blanker monostable. Before the detector is a third IF amplifier with a gain of about 46 dB. The product detector is a double-balanced modulator which operates independently of any other circuits on the chip. In the HF-150 it is used for SSB and synchronous AM reception.

Q32 pin functions. (Levels for USB mode, 50 uV input signal resolved at 1 kHz)

Pin	Name	DC Voltage	Signal	Function
1	AGC dcpl	2.3V	None	RF AGC decoupling pin
2	AGC bias	2.3V	None	RF AGC threshold adjust resistor
3	AMP1 out	3.6V	IF 7mVp-p	1st IF amplifier output
4	AMP2 in	0.8V	IF 4mVp-p	2nd IF amplifier input
5	Del AGC	0.0V	None	AGC to RF stage
6	IF output	4.2V	IF 2mVp-p	2nd IF amplifier output
7	Mixer in	1.5V	IF 25mVp-p	Product detector IF input
	Mixer out	3.7V	Audio 200mVp-p	SSB audio output
9	LO input	1.5V	CAR 200mVp-p	Product detector CAR osc input
10	Vcc	5.0V	None	5V Supply
11	NB out	0.0V	None	Noise blanker monostable output
12	NB timer	0.0V	None	Monostable R/C
13	Det input	0.8V	IF 1.5mVp-p	AM / AGC detector IF input
14	Decoupling	1.5V	None	AM detector decoupling pin
15	Audio out	1.0V	Some audio (<40mV)	AM audio output
16	AGC dcpl	2.3V	None	AGC level output, AGC time constant
17	Gnd	0V	None	Ground connection
18	IF input	0.8V	IF 2mVp-p	1st IF amplifier input

MC3357P FM IF amplifier, Q27.

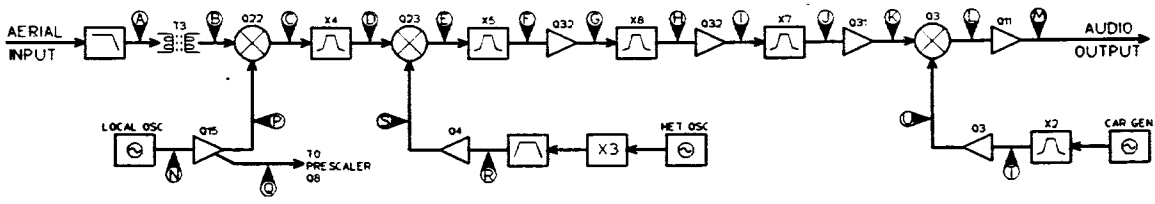


The MC3357P contains an IF conversion mixer, a limiter amplifier and a quadrature FM detector. In the HF-150 the mixer is used as a phase detector for the synchronous AM system, and takes its IF signal from the output of the limiter amplifier. The FM demodulator and squelch circuits are not used.

Q27 pin functions. (Levels for ASD mode, 50uV input signal, unmodulated)

Pin	Name	DC Voltage	Signal	Function
1	Osc input	5.0V	455 kHz 250mVp-p	Carrier signal input
2	Osc output	4.4V	455 kHz 250mVp-p	No connection
3	Mixer out	3.7V	910 kHz 1Vp-p	Sync phase detector output (DC component)
4	Vcc	5.0V	None	5V supply
5	Limiter in	1.0V	IF signal 8mVp-p	455 kHz IF input to limiter amplifier
6	Decoupling	1.0V	None	Limiter amp decoupling pin
7	Limiter out	1.0V	IF 350mVp-p clipped	Limited 455 kHz IF output
8	Quad in	5.0V	None	Tied to Vcc
9	Demod out	2.6V	IF 300mVp-p	No connection
10	Filter in	1.9V	None	Tied to pin 11
11	Filter out	1.9V	None	Tied to pin 10
12	Squelch in	0.0V	None	Tied to ground
13	Squelch out	4.6V	None	No connection
14	Mute	0.0V	None	No connection
15	Gnd	0V	None	Ground connection
16	Mixer in	2.0V	IF 120mVp-p	455 kHz IF input to sync phase detector

Signal levels.



The signal levels shown here can provide a useful fault finding guide to a partially working receiver, however there are a few points to beware of. All signal levels were measured with a high-impedance probe and a frequency selective level meter. The signals at the outputs of mixers are often swamped by oscillator feed-through and so cannot be measured with a broad-band voltmeter.

The specified input signal level of 50 uV drives the AGC system to reduce the gain of the two IF amplifiers but the RF AGC system should still be at full gain. Because of threshold and gain variations within the IF amplifier chip there may be deviations from the stated signal levels in the 455 kHz IF chain without any fault present.

Signal levels and frequencies. Receiver settings :-

Mode	USB
Frequency	14.200 MHz
Aerial Switch	NORM
Input signal	14.201 MHz at 50 uV (-73 dBm) into 50 ohm aerial input.

Point	Connection	Frequency	Level (rms)	Comments
A	Jn L11 / T3		40 uV	Low-pass filter output
B	Q22 pins 12 & 13		85 uV	1st mixer input (same signal on both pins)
C	Q22 pin 3	45.000 MHz	850 uV	1st mixer 45 MHz IF output
D	Q23 pin 13	45.000 MHz	700 uV	45 MHz IF filter output / 2nd mixer input
E	Q23 pin 3	455.4 kHz	1.4 mV	2nd mixer 455 kHz IF output
F	Q32 pin 18	455.4 kHz	360 uV	2.5 kHz filter output
G	Q32 pin 3	455.4 kHz	2.5 mV	1st IF amplifier output
H	Q32 pin 4	455.4 kHz	1.3 mV	X8 filter output
I	Q32 pin 6	455.4 kHz	750 uV	2nd IF amplifier output
J	Jn R107 / R108	455.4 kHz	350 uV	X7 filter output
K	Q32 pin 7	455.4 kHz	8 mV	Product detector input
L	Q32 pin 8	1 kHz	75 mV	Product detector output
M	Test point 6	1 kHz	350 mV	Audio preamplifier output
N	Q15 base	59.201 MHz	300 mV	Local oscillator output
P	Test point 2	59.201 MHz	900 mV	Buffer amplifier output / mixer injection
Q	Q8 pin 2	59.201 MHz	150 mV	Local oscillator feed to PLL prescaler
R	Q24 base	44.5446 MHz	20 mV	HET oscillator tripler output
S	Q23 pin 5	44.5446 MHz	350 mV	HET oscillator mixer injection
T	Jn R7 / R8	456.4 kHz	4 mV	CAR comb filter output
U	Q23 pin 9	456.4 kHz	80 mV	CAR injection to product detector

Test and alignment.

Equipment required :- Frequency counter to operate to 50 MHz.
DVM to measure 10V DC.
HF signal generator with calibrated output.
Audio SINAD meter.

Many of the tests and alignments described here depend on the correct operation and adjustment of other sections of the receiver. It is strongly recommended that this procedure is performed in the order below, and any faults found are rectified before continuing.

The tests listed require the full operating frequency range of the receiver to be available. If the option diode is installed on the control board, restricting coverage, it should be removed before carrying out the testing and alignment and replaced afterwards.

1) Test point function.

TP 1	Local oscillator frequency control voltage.
TP 2	Local oscillator injection to first mixer.
TP 3	B+ supply rail (typically 11V).
TP 4	5V logic and IF supply rail.
TP 5	8V analogue supply rail.
TP 6	Pre-amp audio output.
TP 7	Audio MUTE line (logic high / 5V to mute).
TP 8	Synchronous AM feedback tuning voltage.
TP 9	AGC voltage.

2) Control unit test.

Severe faults in the control system will result in a blank display (no 5V power or faulty display driver) or a display with all segments showing (no microcontroller activity or serial bus fault). If the test routines will run and a malfunction is detected, the display will show the fault symbol **FLT**. The sequence of events before the fault symbol appears can give an indication of the area where the fault was detected.

A fault indication when the receiver is switched on, or during normal operation, is almost certainly due to an internal fault within the microcontroller. Fault indications during test mode generally indicate faults outside the microcontroller.

2.1 Microcontroller function and display driver test.

Switch on the receiver with the **MEM** button pressed, then release the button.
The display should show the **TEST** message if the microcontroller, EEPROM, serial bus and display are functioning correctly. The test routine runs continuously until the **MEM** button is released or an EEPROM fault is detected. This allows bus signals to be monitored with test equipment.

2.2 Frequency memory (EEPROM chip, Q2) test.

If the test indication above is **FLT** instead of **TEST** a problem in the serial bus or EEPROM is likely. Note that the EEPROM is not exhaustively tested, but all essential read and write operations must work for the test to pass. Memories 54 to 60 are preset with frequencies useful for the alignment procedures that follow.

3) Reference oscillator adjustment.

3.1 With the **TEST** message displayed, press the **MODE** button.
Connect a frequency counter to **TP2** (Local Osc).

3.2 Adjust **TC1** (on the control unit) for a reading of 45.00000 MHz +/- 20 Hz.

If a stable 45 MHz cannot be obtained check the reference frequency on Q7 pin 13 which should be 2912.0 kHz. If this is correct, then the local oscillator, PLL or its control system is at fault.
To aid fault finding on the PLL control system, PLL programming data is continuously sent to Q7 whilst the **MODE** button is held pressed.

4) Heterodyne oscillator adjustment.

4.1 With the **TEST** message displayed, connect a frequency counter to **TP6** (Audio).

4.2 Press the **MODE** button.
Adjust **TC2** for a reading of 3234 Hz +/- 10 Hz.

4.3 Press the **FAST** button.
Adjust **VR1** for a reading 8 Hz above that in (4.2) above.

4.4 Repeat (4.2) and (4.3).

The remaining alignment procedures require the receiver to operate in its normal mode. Switch the receiver off and on again to exit test mode.

5) Local oscillator adjustment.

The only adjustment in the local oscillator is the physical layout of the windings on the oscillator coil **T1**. The coil is factory aligned and then potted in hot-melt adhesive - it is unlikely that any further adjustment will be necessary. It is suggested that the following functional checks are made, and the adjustments only performed if absolutely necessary.

5.1 Local oscillator alignment test.

This test should be performed with the metal shield in place around and below the oscillator circuit. Following the frequency memory test above, the receiver frequencies used in this test are programmed into the memory numbers shown.

Connect a DVM between the negative terminal of C28 and **GROUND**.
Check that the voltage is about -2V (ie below ground potential).

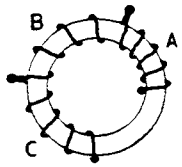
5.2 Re-connect the DVM between **TP1** (VCO control) and **GROUND**.
Check the voltage on TP1 for receiver frequency settings shown below:-

Frequency	Memory	TP2 Voltage
29.990 MHz		less than 7.1 V
11.578 MHz		more than 1.5 V
11.574 MHz		less than 7.1 V
30 kHz		more than 1.5 V

5.3 Local oscillator coil adjustment.
Use a hot air gun to soften the potting compound around the coil.

Oscillator coil T1 sections.

A = 5 turns
B = 4 turns
C = 4 turns



Refer to the checks in section (5.2), adjusting the turn spacing in section A for the voltage at 29.990 MHz, and section C for 11.574 MHz. If possible set these voltages at 6.7 V, checking that the low voltages specified in (5.2) do not fall below 1.5 V. If the limits cannot be met then slide the turns in section B of the coil towards the C section, and repeat the adjustments. Continued failure would suggest faulty components D5 or Q13.

When adjustments are complete, check that the potting securely holds all turns on the coil. Carry out the checks (5.2) again when the coil and circuit has returned to room temperature.

6) I F alignment.

The only adjustment in the I F section is the physical layout of the windings on the first mixer output transformer T4. The coil is factory aligned and it is unlikely that any further adjustment will be necessary unless components around it are replaced. Correct alignment requires a two-signal source to measure the intermodulation performance of the receiver, and no adjustment should be made unless signal generators and a hybrid combiner of sufficient performance are available.

If the following sensitivity test (6.1 / 6.2 / 6.3) is successful and T4 has not been disturbed then no adjustment should be necessary.

6.1 Connect a signal generator to the 50 ohm aerial input socket.
Set the aerial select switch to **NORM**
Inject 5 uV (-93 dBm) at 29.990 MHz modulated with 70% AM at 1kHz.
Tune the receiver to 29.990 MHz AM (memory 59).

Check that the receiver resolves the input signal at 1kHz.

6.2 Connect a SINAD meter to the EXT LS socket.
Set the volume control to mid-position.
Reduce the signal generator output to 1 uV (-107 dBm).

Check that the SINAD reading is greater than 10 dB.

6.3 Set the signal generator frequency to 500 kHz, and re-tune the receiver (memory 56).

Check that the SINAD reading is greater than 10 dB.

6.4 With the receiver setup as in (6.2) or (6.3) adjust the turns spacing on T4 to maximise the SINAD meter reading. Try to keep the configuration of T4 as symmetric as possible about the centre-tap.

6.5 Connect two signal generators via a combining unit and a 10 dB attenuator to the 50 ohm aerial input socket.
Set the generator frequencies to 14.315 MHz and 14.365 MHz, unmodulated, and adjust the output levels so that both signals are at -30 dBm at the receiver input.
Tune the receiver to 14.264 MHz, USB (memory 54 on V1.3 onwards).
Connect a SINAD meter to the EXT LS socket.
Set the volume control to mid-position.
Fine tune the receiver to resolve the output at 1kHz (ie for maximum SINAD reading).

Adjust the symmetry of turns on **T4** to minimise the SINAD reading. Only a small adjustment should be necessary to one half of the transformer. If a large adjustment is needed, the sensitivity tests (6.1 / 6.2 / 6.3) should be repeated to make sure that the transformer has not been de-tuned.

7) Input filter alignment.

7.1 Connect a signal generator to the 50 ohm antenna input socket.
Set the aerial select switch to **NORM**
Inject 5 mV (-33 dBm) at 45.000 MHz modulated with 70% AM at 1kHz.
Tune the receiver to 29.990 MHz, AM (memory 59)
Connect a SINAD meter to the EXT LS socket.
Set the volume control to mid-position.

Adjust **TC3** for minimum SINAD reading.
Early receivers have a small fixed capacitor connected across C54 instead of TC3. The value of this extra capacitor can be changed to null the 45 MHz response if the SINAD reading is higher than 15 dB.

8) Whip amplifier test.

8.1 Connect a signal generator to the 50 ohm aerial input socket.
Set the aerial select switch to **WHIP**
Inject 5 uV (-93 dBm) at 29.990 MHz modulated with 70% AM at 1kHz.
Tune the receiver to 29.990 MHz AM (memory 59).

Check that the receiver resolves the input signal at 1kHz.

8.2 Connect a SINAD meter to the EXT LS socket.
Set the volume control to mid-position.
Reduce the signal generator output to 0.3 uV (-117 dBm).

Check that the SINAD reading is greater than 10 dB.

8.3 Set the signal generator frequency to 500 kHz, and re-tune the receiver (memory 56).

Check that the SINAD reading is greater than 10 dB.

Disassembly.

To remove the top case of the receiver proceed as follows :-

Undo four screws on the underside of the receiver and remove the bottom plate.
Undo four screws underneath, fastening the circuit board to the case.
Remove the two outside screws holding the battery cases on the rear panel.
Remove the upper right-hand screw from the display window, and the screw opposite this on the rear panel.
Remove the eight socket-head screws holding front and rear panels to the case.
Lift the right-hand edge of the case about 15mm, and slide the case to the left. Then lift the left-hand edge of the case clear of the receiver.

The battery cases can be removed to give access to the main PCB by removing the remaining two securing screws and sliding the cases out of the panel. The battery wiring need not be unconnected unless the rear panel has to be removed. Separating the top case by unsoldering the connecting wires from the loudspeaker is recommended to prevent damage to the finish.

If access is required to components on the control board, the front panel can be separated by removing the volume and tuning knobs, and then undoing the countersunk screw behind the tuning knob. The window can remain attached to the panel.

Parts list. Control Unit

Component	Type / Value	Part No.
C 1	Ceramic plate N150 22pF 100V	C02-2200
C 2	Ceramic plate N150 27pF 100V	C02-2700
C 3	Axial electrolytic 4.7uF 63V	E16-4790
C 4,5	Box polyester 22nF 100V	C31-2232
C 6-8	Multilayer Ceramic Z5U 100nF 50V	C23-1040
C 9	Ceramic plate high K 22nF 63V	C21-2230
C 10	Ceramic plate N750 220pF 100V	C03-2210
	Signal diode 1N4148	D01-4148
J 1,2	25-way SIL socket for LCD	N12-0251
LCD 1	6 digit x 12.5mm LCD	O21-1260
Q 1	Microcontroller (for HF-150) S83C751	Z90-1513
Q 2	128 x 16bit serial EEPROM ST93CS56	Z21-9356
Q 3	NPN transistor BC183L	Q01-1831
Q 4	Programmable divider MC14569BCP	Z12-0069
Q 5	Dual D-type latch 74HC74	Z06-0074
Q 6	LCD driver MM5453N	Z23-5453
R 1	Carbon film 1/8W 5% 1k0	R01-1020
R 2-5	Carbon film 1/8W 5% 47k	R01-4730
R 6	Carbon film 1/8W 5% 10k	R01-1030
R 7	Carbon film 1/8W 5% 1k5	R01-1520
R 8	Carbon film 1/8W 5% 1M0	R01-1050
R 9	Carbon film 1/8W 5% 4k7	R01-4720
R 10	Carbon film 1/8W 5% 1k0	R01-1020
R 11	Carbon film 1/8W 5% 100R	R01-1010
R 12	Carbon film 1/8W 5% 22k	R01-2230
S 1-3	Push button, black	S23-0010
S 4	Mechanical encoder 2 phase, 50 pulse	S31-5020
	Film trimmer cap 2 to 10pF	C42-1000
X 1	Quartz crystal 11.648 MHz	X01-1130
X 2	455 kHz filter 6 kHz b/w CFW455HT	X23-6090

Main Unit

C 11,12	Ceramic plate high K 22nF 63V	C21-2230
C 13	Radial electrolytic 10uF 35V	E04-1000
C 14,15	Ceramic plate medium K 1nF 100V	C11-1020
C 16	Box polyester 1uF 63V	C31-1051
C 17	Box polyester 100nF 63V	C31-1041
C 18	Multilayer Ceramic Z5U 100nF 50V	C23-1040
C 19,20	Ceramic plate medium K 1nF 100V	C11-1020
C 21	Ceramic plate high K 22nF 63V	C21-2230
C 22	Ceramic plate N150 33pF 100V	C02-3300
C 23	Ceramic plate NP0 10pF 100V	C01-1000
C 24	Ceramic plate high K 22nF 63V	C21-2230
C 25	Radial electrolytic 220uF 10V	E01-2212
C 26	Radial electrolytic 10uF 35V	E04-1000
C 27	Ceramic plate high K 22nF 63V	C21-2230
C 28	Radial electrolytic 2u2 63V	E06-2290
C 29	Ceramic plate N150 150pF 100V	C02-1510
C 30,31	Multilayer Ceramic Z5U 100nF 50V	C23-1040
C 32	Radial electrolytic 2u2 63V	E06-2290
C 33	Ceramic plate high K 22nF 63V	C21-2230
C 34	Ceramic plate NP0 10pF 100V	C01-1000
C 35	Ceramic plate N150 22pF 100V	C02-2200
C 36	Ceramic plate N150 47pF 100V	C02-4700
C 37	Ceramic plate high K 22nF 63V	C21-2230
C 38,39	Ceramic plate NP0 2p2 100V	C01-2290
C 40	Ceramic plate NP0 6p8 100V	C01-6890
C 41	Ceramic plate N750 220pF 100V	C03-2210
C 42	Miniature Radial electrolytic 1000uF 16V	E22-1023
C 43	Radial electrolytic 220uF 16V	E02-2213
C 44	Multilayer Ceramic Z5U 100nF 50V	C23-1040
C 45	Ceramic plate high K 10nF 63V	C21-1030
C 46-48	Radial electrolytic 100uF 10V	E01-1011
C 49	Multilayer Ceramic Z5U 100nF 50V	C23-1040
C 50	Box polyester 100nF 63V	C31-1041
C 51	Ceramic plate high K 10nF 63V	C21-1030
C 52	Multilayer Ceramic Z5U 100nF 50V	C23-1040
C 53,54	Ceramic plate N150 47pF 100V	C02-4700
C 55,56	Ceramic plate N750 220pF 100V	C03-2210
C 57	Ceramic plate NP0 10pF 100V	C01-1000
C 58	Ceramic plate NP0 4p7 100V	C01-4790

C 59	Ceramic plate medium K 1nF 100V	C11-1020
C 60	Ceramic plate NP0 10pF 100V	C01-1000
C 61	Multilayer Ceramic Z5U 100nF 50V	C23-1040
C 62	Ceramic plate NP0 4p7 100V	C01-4790
C 63	Ceramic plate N150 39pF 100V	C02-3900
C 64	Ceramic plate N150 150pF 100V	C02-1510
C 65	Miniature Radial electrolytic 470uF 16V	E22-4713
C 66-69	Ceramic plate high K 22nF 63V	C21-2230
C 70	Multilayer Ceramic Z5U 100nF 50V	C23-1040
C 71	Radial electrolytic 10uF 35V	E04-1000
C 72,73	Ceramic plate high K 22nF 63V	C21-2230
C 74,75	Ceramic plate medium K 1nF 100V	C11-1020
C 76,77	Ceramic plate high K 22nF 63V	C21-2230
C 78	Ceramic plate high K 10nF 63V	C21-1030
C 79,80	Box polyester 100nF 63V	C31-1041
C 81	Radial electrolytic 10uF 35V	E04-1000
C 82	Box polyester 22nF 100V	C31-2232
C 83	Radial electrolytic 2u2 63V	E06-2290
C 84	Radial electrolytic 10uF 35V	E04-1000
C 85	Radial electrolytic 47uF 25V	E03-4701
C 86	Box polyester 100nF 63V	C31-1041
C 87	Miniature radial electrolytic 470uF 10V	E21-4712
C 88	Multilayer Ceramic Z5U 100nF 50V	C23-1040
C 89,90	Ceramic plate high K 22nF 63V	C21-2230
C 91	Ceramic plate N750 220pF 100V	C03-2210
C 92,93	Ceramic plate medium K 1nF 100V	C11-1020
C 94	Ceramic plate N150 33pF 100V	C02-3300
C 95	Ceramic plate medium K 1nF 100V	C11-1020
C 96	Ceramic plate medium K 2n2 100V	C11-2220
C 97,98	Miniature radial electrolytic 470uF 10V	E21-4712
C 99,100	Ceramic plate high K 10nF 63V	C21-1030
C 101	Ceramic plate high K 22nF 63V	C21-2230
C 102	Ceramic plate high K 10nF 63V	C21-1030
C 103	Radial electrolytic 10uF 35V	E04-1000
C 104-107	Multilayer Ceramic Z5U 100nF 50V	C23-1040
C 108	Ceramic plate N750 220pF 100V	C03-2210
C 109	Box polyester 100nF 63V	C31-1041
C 110	Ceramic plate high K 10nF 63V	C21-1030
C 111	Box polyester 100nF 63V	C31-1041
C 112	Radial electrolytic 10uF 35V	E04-1000
C 113	Ceramic plate medium K 4n7 100V	C11-4720
C 114	Ceramic plate medium K 2n2 100V	C11-2220
D 3,4	Varicap diode BB90A9	D03-0909
D 5	PIN switching diode BA482 (BA244A)	D02-0482
D 6-9	Signal diode 1N4148	D01-4148
D 10-13	High speed diode BAW62	D02-0062
D 14-16	Rectifier diode 1N4002	D01-4002
D 17	PIN attenuator diode MI204	D31-0204
D 18-28	Signal diode 1N4148	D01-4148
J 3	PCB power socket, 2.1mm	J13-2193
J 4	2-way 0.1" wafer, non locking	N01-0020
J 5,8,10	PCB jack socket, 3.5mm mono	J11-3593
J 6	Red & black spring terminal block	J21-0010
J 7	Two hole flange mount SO-239	J01-2390
J 9	PCB jack socket, 6.5mm stereo	J11-0602
L 1,3	Ferrite axial inductor 1mH	L01-1023
L 2	Ferrite axial inductor 3u3	L01-3392
L 4	Ferrite axial inductor 47uH	L01-4702
L 5,8	Ferrite axial inductor 1uH	L01-1092
L 6,7	Ferrite axial inductor 1mH	L01-1023
L 9-11	Ferrite axial inductor 270nH	L01-2782
L 12-19	Ferrite axial inductor 1mH	L01-1023
Q 7	PLL synthesiser system TDD1742T	U44-1742
Q 8	Dual modulus prescaler uPB553AC	Z31-0553
Q 9,10	Shift & store register 74HC4094 (sop)	Z07-4094
Q 11	Quad BiFET op-amp TL064CM (sop)	U42-1064
Q 12	PNP transistor BC212L	Q01-2121
Q 13,14	N channel junction FET J310	Q14-0310
Q 15	NPN RF transistor ZTX327	Q16-0327
Q 16	Voltage regulator, 5V 78L05	U23-0050
Q 17	Voltage regulator, LP2951CM (sop)	U24-0011
Q 18	Quad analogue switch 4066 (sop)	Z11-1066
Q 19	N channel junction FET J310	Q14-0310
Q 20,21	NPN transistor BC183L	Q01-1831
Q 22,23	High level mixer SL6440CDP	U12-6440
Q 24	NPN RF transistor ZTX320	Q16-0320
Q 25	Audio amplifier TDA1904	U43-1904
Q 26	Quad NOR gate 74HC02 (sop)	Z07-0002
Q 27	FM IF system MC3357P	U13-3357
Q 28-31	NPN transistor BC183L	Q01-1831
Q 32	IF amp & detector SL6700CDP	U12-6700
R 13	Carbon film 1/8W 5% 100k	R01-1040
R 14,15	Carbon film 1/8W 5% 220k	R01-2240
R 16	Carbon film 1/8W 5% 4M7	R01-4750
R 17	Carbon film 1/8W 5% 47k	R01-4730
R 18,19	Carbon film 1/8W 5% 4k7	R01-4720
R 20	Carbon film 1/8W 5% 47k	R01-4730
R 21	Carbon film 1/8W 5% 470R	R01-4710
R 22	Carbon film 1/8W 5% 1k0	R01-1020
R 23	Carbon film 1/8W 5% 220R	R01-2210
R 24	Carbon film 1/8W 5% 100R	R01-1010
R 25	Carbon film 1/8W 5% 470R	R01-4710
R 26	Carbon film 1/8W 5% 68k	R01-6830
R 27	Carbon film 1/8W 5% 220R	R01-2210
R 28	Carbon film 1/8W 5% 47k	R01-4730
R 29	Carbon film 1/8W 5% 100k	R01-1040
R 30	Carbon film 1/8W 5% 22k	R01-2230
R 31	Carbon film 1/8W 5% 68k	R01-6830
R 32	Carbon film 1/8W 5% 100k	R01-1040
R 33	Carbon film 1/8W 5% 22k	R01-2230
R 34	Carbon film 1/8W 5% 100k	R01-1040
R 35	Carbon film 1/8W 5% 2M2	R01-2250
R 36	Carbon film 1/8W 5% 220k	R01-2240
R 37	Carbon film 1/8W 5% 10k	R01-1030
R 38	Metal film 3/8W 1% 7k50	R11-7520
R 39	Metal film 3/8W 1% 15k0	R11-1530
R 40	Metal film 3/8W 1% 30k0	R11-3030
R 41-43	Carbon film 1/8W 5% 120k	R01-1240
R 44	Carbon film 1/8W 5% 240k	R01-2440
R 45	Carbon film 1/8W 5% 470k	R01-4740
R 46	Metal film 3/8W 1% 3k30	R11-3320
R 47	Metal film 3/8W 1% 13k0	R11-1330
R 48	Metal film 3/8W 1% 15k0	R11-1530
R 49	Carbon film 1/8W 5% 1k0	R01-1020
R 50	Carbon film 1/8W 5% 330R	R01-3310
R 51	Carbon film 1/8W 5% 4k7	R01-4720
R 52	Carbon film 1/8W 5% 2k2	R01-2220
R 53	Carbon film 1/8W 5% 1M0	R01-1050
R 54	Carbon film 1/8W 5% 1k5	R01-1520
R 55,56	Metal film 3/8W 1% 120R	R11-1210
R 57	Metal film 3/8W 1% 15k0	R11-1530
R 58	Metal film 3/8W 1% 82k0	R11-8230
R 59,60	Metal film 3/8W 1% 39R0	R11-3900
R 61	Carbon film 1/8W 5% 2k2	R01-2220
R 62	Carbon film 1/8W 5% 68k	R01-6830
R 63	Carbon film 1/8W 5% 220k	R01-2240
R 64	Carbon film 1/8W 5% 100k	R01-1040
R 65	Carbon film 1/8W 5% 4k7	R01-4720
R 66	Carbon film 1/8W 5% 56R	R01-5600
R 67	Carbon film 1/8W 5% 470R	R01-4710
R 68	Carbon film 1/8W 5% 100k	R01-1040
R 69	Carbon film 1/8W 5% 10R	R01-1000
R 70	Carbon film 1/8W 5% 150R	R01-1510
R 71,72	Carbon film 1/8W 5% 1k5	R01-1520
R 73	Carbon film 1/8W 5% 56R	R01-5600
R 74,75	Carbon film 1/8W 5% 330R	R01-3310
R 76	Carbon film 1/8W 5% 10k	R01-1030
R 77	Carbon film 1/8W 5% 47k	R01-4730
R 79,80	Carbon film 1/8W 5% 220R	R01-2210
R 81	Carbon film 1/8W 5% 470R	R01-4710
R 82	Carbon film 1/8W 5% 2k2	R01-2220
R 83	Carbon film 1/8W 5% 1k5	R01-1520
R 84	Carbon film 1/8W 5% 220k	R01-2240

R 85	Carbon film 1/8W 5% 68k	R01-6830
R 86	Carbon film 1/8W 5% 47k	R01-4730
R 87	Carbon film 1/8W 5% 220k	R01-2240
R 88	Carbon film 1/8W 5% 4k7	R01-4720
R 89	Carbon film 1/8W 5% 10k	R01-1030
R 90	Carbon film 1/8W 5% 470R	R01-4710
R 128	Carbon film 1/8W 5% 100R	R01-1010
R 91	Carbon film 1/8W 5% 3R3	R01-3390
R 92,93	Carbon film 1/8W 5% 220R	R01-2210
R 94	Carbon film 1/8W 5% 22k	R01-2230
R 95	Carbon film 1/8W 5% 100k	R01-1040
R 96	Carbon film 1/8W 5% 220k	R01-2240
R 97	Carbon film 1/8W 5% 47k	R01-4730
R 98	Carbon film 1/8W 5% 10k	R01-1030
R 99	Carbon film 1/8W 5% 4k7	R01-4720
R 100	Carbon film 1/8W 5% 220k	R01-2240
R 101	Carbon film 1/8W 5% 22k	R01-2230
R 102	Carbon film 1/8W 5% 220k	R01-2240
R 103	Carbon film 1/8W 5% 56R	R01-5600
R 104	Carbon film 1/8W 5% 220R	R01-2210
R 105	Carbon film 1/8W 5% 47k	R01-4730
R 106	Carbon film 1/8W 5% 1k5	R01-1520
R 107	Carbon film 1/8W 5% 1M0	R01-1050
R 108	Carbon film 1/8W 5% 1k5	R01-1520
R 109,111	Carbon film 1/8W 5% 10k	R01-1030
R 110,112	Carbon film 1/8W 5% 4k7	R01-4720
R 113	Carbon film 1/8W 5% 2k2	R01-2220
R 114,115	Carbon film 1/8W 5% 100R	R01-1010
R 116	Carbon film 1/8W 5% 2k2	R01-2220
R 117,118	Carbon film 1/8W 5% 100R	R01-1010
R 119	Carbon film 1/8W 5% 2k2	R01-2220
R 120	Carbon film 1/8W 5% 100k	R01-1040
R 121	Carbon film 1/8W 5% 1k5	R01-1520
R 122	Carbon film 1/8W 5% 470R	R01-4710
S 5	Miniature r/a slide switch 2-pole 3-way	S03-0320
T 1	RF toroidal coil 5+4+4 turns	L21-0030
T 2,3	RF transformer 4 : 14 turns	L21-0010
T 4	RF toroidal coil 5 + 5 turns	L21-0020
TC 2	Film trimmer cap 1p0 to 5p5	C42-5590
TC 3	Ceramic trimmer cap 1p5 to 5p0	C41-5090
VR 1	Sub-min horizontal preset 470R	G11-4710
VR 2	16mm pot + DPDT switch 20kA (log)	G04-2030
X 3	Quartz crystal 14.8483 MHz	X01-1430
X 4	45 MHz x-tal filter 15 kHz b/w (two pcs)	X11-4500
X 5	455 kHz filter 2.5 kHz b/w CFJ455K5	X24-2590
X 6	455 kHz filter 6 kHz b/w CFW455HT	X23-6090
X 7,8	455 kHz filter 6 kHz b/w CFU455HT	X22-6090
	Local oscillator screening box	H12-0790

Case Assembly

Case extrusion	H11-0830
Case bottom panel	H11-0860
Case feet	H22-0060
Case front panel	H01-0850
Case rear panel	H01-0870
Foam padding, 2mm thick	F23-0010
Foam padding, 8mm thick	F23-0040
Loudspeaker, 80mm 8 ohms	T11-0801
Battery holder	H31-0810
Display window	H11-0840
15mm knob, VOLUME	K01-0150
Black cap for knob	K03-2150
40mm knob, TUNING	K15-0890
Hexagonal pillar 10mm x M3	F12-3100
M2.5 x 5mm screw, black	F01-2551
M2.5 x 10mm screw, black	F01-2511
M3 x 6mm screw, taptite, black	F03-3061
M3 x 6mm screw, c/s taptite, black	F04-3061
M3 x 10mm screw, black	F01-3101
M3 x 16mm screw, taptite, black	F03-3161
M4 x 10mm button head socket screw	F08-4101
M5 x 12mm screw, countersunk, black	F02-5121
M5 half nut (for case feet)	F11-5001

Accessories

12V power supply (240V mains)	A02-0120
Carton	P01-1500
Packing material	P01-1501
	P01-1502
Colour wrap	P02-1500
User manual	M01-1500
Technical manual	M02-1500

Options. KPAD-1 keypad.

C 1	Box polyester 33nF 100V	C31-3332
C 2,4	Radial electrolytic 22uF 16V	E02-2200
C 3	Radial electrolytic 100uF 10V	E01-1010
D 1	Signal diode 1N4148	D01-4148
J 3	3.5mm jack plug, plastic shell	J12-3593
Q 1	Keypad PPM generator SL490BDP	U12-0490
Q 2	Voltage regulator, 8V 78L08	U23-0080
Q 3,4	NPN transistor BC183L	Q01-1831
R 1	Metal film 1/4W 1% 68.0k	R12-6830
R 2	Carbon film 1/8W 5% 2k2	R01-2220
R 3	Carbon film 1/8W 5% 100k	R01-1040
R 4	Carbon film 1/8W 5% 22k	R01-2230
R 5	Carbon film 1/8W 5% 150R	R01-1510
S 1	12-key numeric keypad, 4 x 3 matrix	S32-1210
	Cable tie for strain relief	F22-0920
	Keypad case assembly	H21-0470
	Cable exit panel	H20-0470
	Adhesive feet, 7mm dia	H22-0030
	Keypad cable, 750mm	W11-6090

IF-150 Computer interface.

C 1	Ceramic cap Y5V 470nF 25V SM1206	C53-4741
C 2,3	Ceramic cap C0G 22pF 50V SM0805	C51-2200
C 4	SM electrolytic 22uF 16V	E32-2205
C 5,6	Ceramic cap X7R 220pF 50V SM0805	C52-2210
D 1	Signal diode BAS16	D02-0016
J 1	25-way D-type female connector	J32-0250
J 2	3.5mm jack plug, plastic shell	J12-3593
L 1	Ferrite inductor 100uH SM1812	L03-1010
Q 1	Optoisolator IL213 (sop)	U45-0213
Q 2	Microcontroller (for IF150) S87C751	Z24-7751
Q 3	Voltage regulator, 5V 78L05 (sop)	U23-0051
Q 4	NPN transistor BCW33	Q01-0330
R 1	Chip resistor 3k3 1/8W 5% SM0805	R51-3320
R 2,3	Chip resistor 10k 1/8W 5% SM0805	R51-1030
R 4	Chip resistor 150R 1/8W 5% SM0805	R51-1510
X 1	Quartz crystal 8 MHz HC49/4H	X01-0831
	Connector cover	J35-1250
	Connection cable, 2m	W11-6090
	Cable sleeve	F22-0300
	Cable tie for strain relief	F22-0920
	Instruction sheet	M03-1500

Receiver specification.

Description.

Frequency coverage	30 kHz to 30 MHz continuous coverage. (150 kHz to 30 MHz) **
Reception modes	LSB, USB, AM, Synchronous AM (USB, LSB, DSB).
Receiver system	Microprocessor controlled PLL tuning, dual conversion superheterodyne receiver. First intermediate frequency 44.999 MHz to 45.000 MHz. Second intermediate frequency 455 kHz.
Display	5-digit LCD showing receiver frequency to the nearest kilohertz. The LCD also shows memory numbers and receiver mode when appropriate.
Tuning	By spin-wheel and direct keypad frequency entry. ** Tuning rates :- SSB and AM Sync modes - 8 Hz steps, 1.6 kHz per revolution. AM mode - 60 Hz steps, 12 kHz per revolution. Tuning step size increases with rapid spin-wheel rotation. Keypad frequency entry is to 1 kHz resolution. FAST mode spin-wheel tunes to nearest 100 kHz at 5MHz per revolution.
Memories	60 memories holding frequency and mode, selected with tuning spin-wheel or keypad. ** Data held in EEPROM for > 10 years. Memory functions : Store, Recall, and Preview. Receiver operating frequency and mode is retained while switched off.
I F filters	SSB, AM narrow and AM Sync (USB/LSB) : 2.5 kHz. AM, AM Sync (DSB) : 7 kHz.
R F attenuator	Operator selectable 20 dB attenuator.
Controls	Power on/off and Volume control. Memory select button. Mode select button - LSB, USB, AMN, AM, ASD, ASF, ASL, ASU. Fast tune button. Tuning / memory select spin-wheel. Aerial select switch (on rear panel) - Whip aerial / 50 ohm aerial / Attenuator.
Aerial inputs	50 ohm input via SO-239 socket. 600 ohm input and Earth connection on spring terminals. High-impedance active aerial input for whip antenna via SO-239 socket.
Audio outputs	Record output at approx 200 mV (3.5mm jack socket). External loudspeaker (3.5mm jack socket). Headphone output (mono or stereo headphones) (6.3mm jack socket). The internal loudspeaker is disconnected when headphones or an external LS are plugged in.
Power supply	External 12V DC supply (2.1mm power jack). 240V AC Mains power unit supplied as standard. Internal batteries (8 AA-size cells) with charging circuit included for NiCd cells.
Dimensions	Size 185 x 80 x 175 mm (WxHxD, overall). Weight approx 1.3 kg (1.5 kg with batteries).

** Indicates facility available if appropriate option is fitted.

Performance.

Sensitivity

Signal levels are in micro-volts (uV) PD across the 50 ohm aerial input.
Sensitivity measured with 10 dB signal/noise ratio at the receiver output.
AM signal modulated 70% at 1 kHz, SSB signal unmodulated, resolved at 1 kHz.

50 kHz to 500 kHz	AM	less than 2 uV.
	SSB	less than 1 uV.
500 kHz to 30 MHz	AM	less than 1 uV. typically 0.3 uV with whip aerial selected.
	SSB	less than 0.5 uV. typically 0.2 uV with whip aerial selected.

Selectivity

Narrow filter :-	2.6 kHz at -6 dB	shape factor 1 : 1.6
	4.1 kHz at -60 dB	
Wide filter :-	6.5 kHz at -6 dB	shape factor 1 : 1.6
	10.2 kHz at -60 dB	

Dynamic range

Reciprocal mixing effects :- (with 2.5 kHz filter)
More than 75 dB at 5 kHz from wanted signal.
More than 85 dB at 10 kHz from wanted signal
More than 100 dB at > 100 kHz from wanted signal

Intermodulation effects :- (with 2.5 kHz filter)
At 10 kHz signal separation : 3rd order intercept point > -20 dBm
Intermodulation-free dynamic range > 70 dB
At 20 kHz signal separation : 3rd order intercept point > +4 dBm
Intermodulation-free dynamic range > 85 dB
At 50 kHz signal separation : 3rd order intercept point > +7 dBm
Intermodulation-free dynamic range > 90 dB

Spurious responses

Images :-	At + 90 MHz	more than 65 dB rejection
	At + 910 kHz	more than 65 dB rejection
Fixed :-	At 45 MHz	more than 70 dB rejection
	At 455 kHz	more than 70 dB rejection

Frequency stability

(Typical performance only - not guaranteed spec)

At constant 20 C	Drift < +/- 30 Hz in one hour
	Frequency error < +/- 50 Hz
-10 C to +50 C	Frequency error < +/- 200 Hz

Audio output

1.6 W into 8 ohms at 5% THD (With supplied 12V power unit).
2.0 W into 4 ohms at 5% THD (With supplied 12V power unit).
External LS output is suitable for loudspeakers with impedances of 4 ohms or greater.
Headphone output : up to 4 Volts from 220 ohms.
Record output : 200 mV from 5 kohms.

Frequency response

SSB mode :	370 Hz to 2.5 kHz (-6dB)	
AM mode :	70 Hz to 3.6 kHz (-6dB)	
ASF mode :	70 Hz to 4.5 kHz (-6dB)	at LS output
	25 Hz to 4.5 kHz (-6dB)	at record output

Distortion

AM mode : 1 kHz signal modulated at 70% depth.
With standard AM detector : THD < 1.5%
With synchronous detector : THD < 0.8%

SSB mode : 1kHz resolved signal THD < 0.8%
Two-signal IM products > 35 dB below wanted,
with signal separation > 200 Hz.

AMS Detector

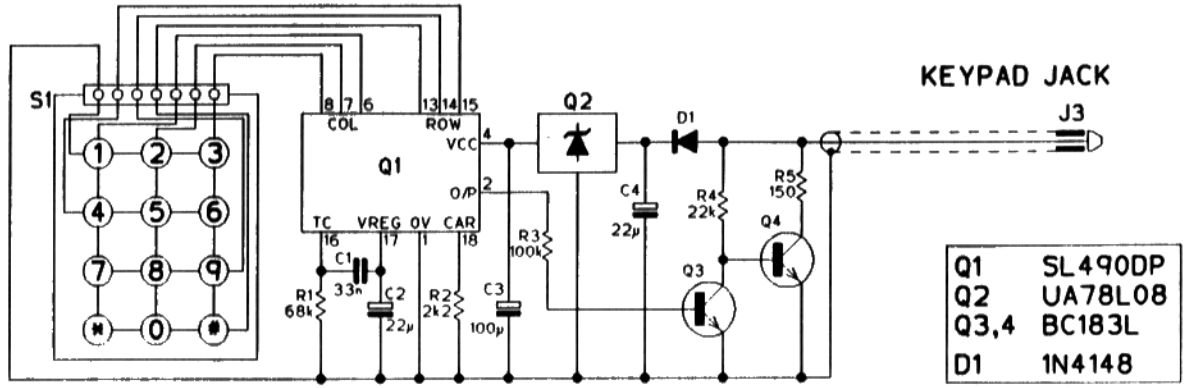
Lock range : DSB +/- 100 Hz, SSB +/- 50 Hz
Audio distortion under carrier-fade conditions. Signal modulated to 70% wrt full carrier level.

6 dB carrier reduction :	1.1% THD	(15% with conventional AM detector).
10 dB carrier reduction :	1.6% THD	(30% with conventional AM detector).
20 dB carrier reduction :	3.9% THD	(50% with conventional AM detector).

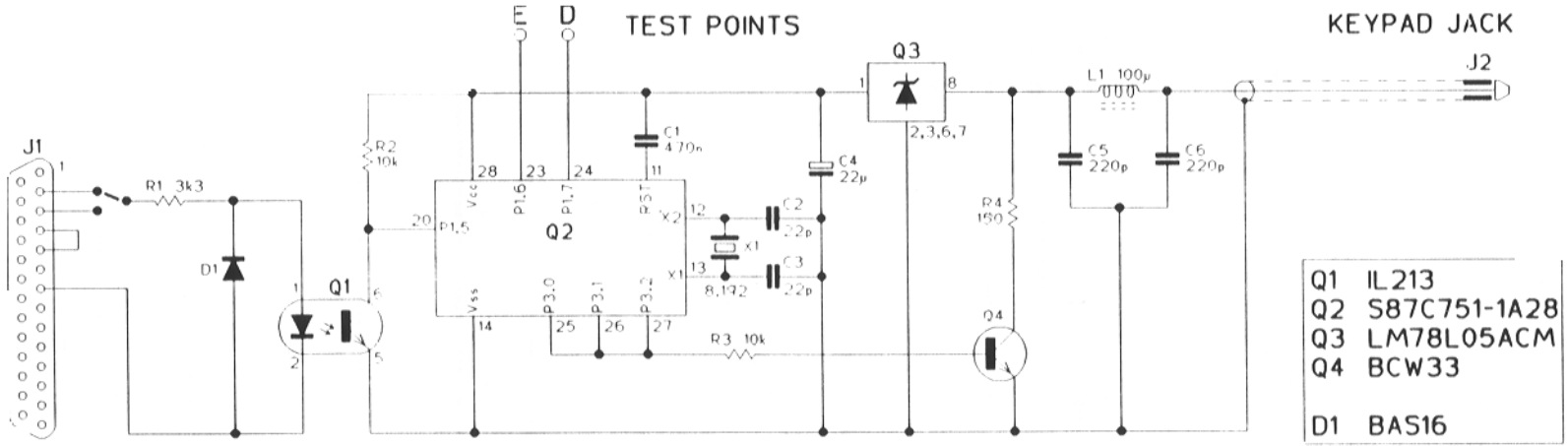
Power supply

DC supply 10 to 15 V (12 V nominal).
Quiescent current 130 mA (no audio output).
Typical power consumption 150 to 300 mA.

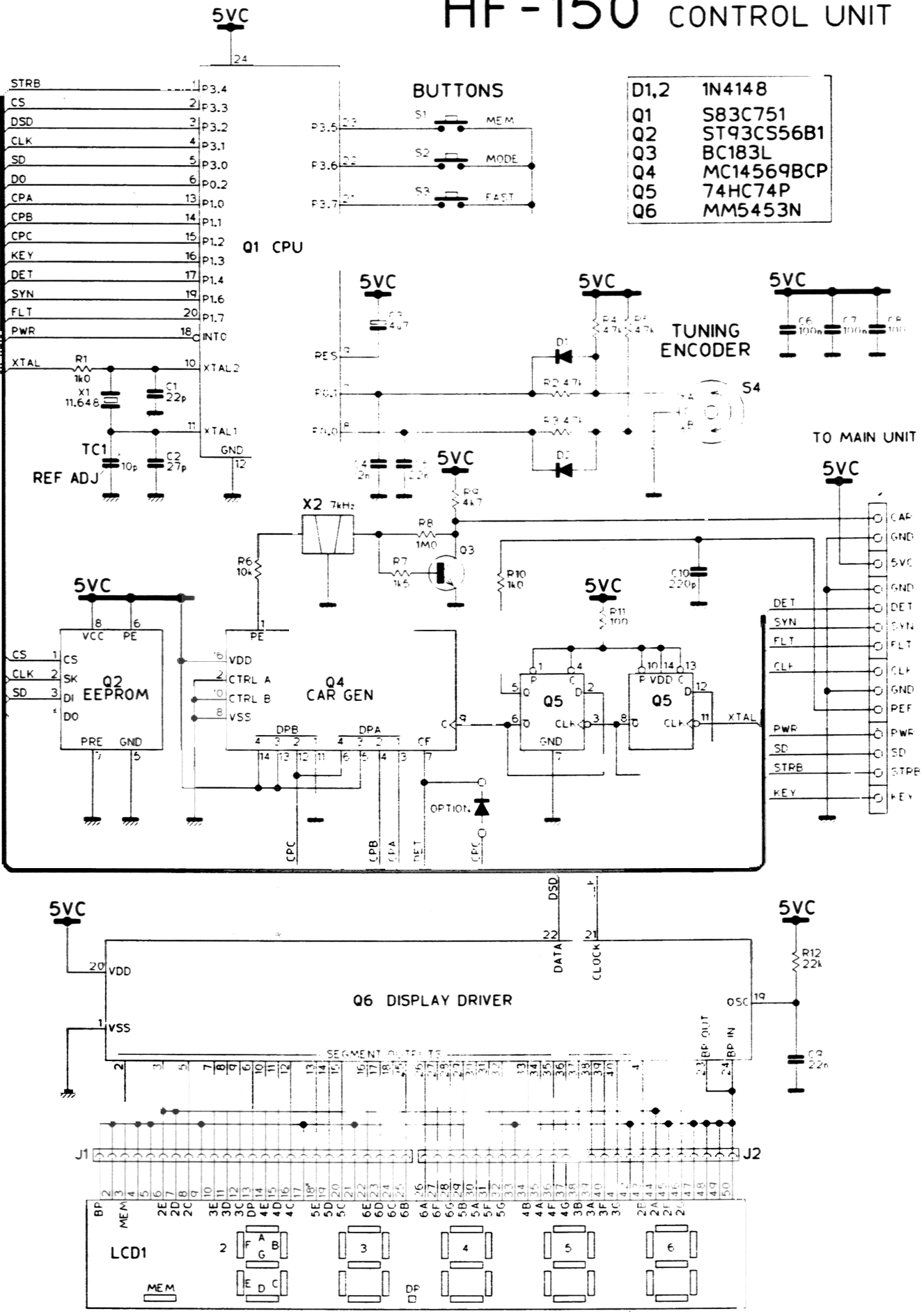
Specification subject to change without notice.

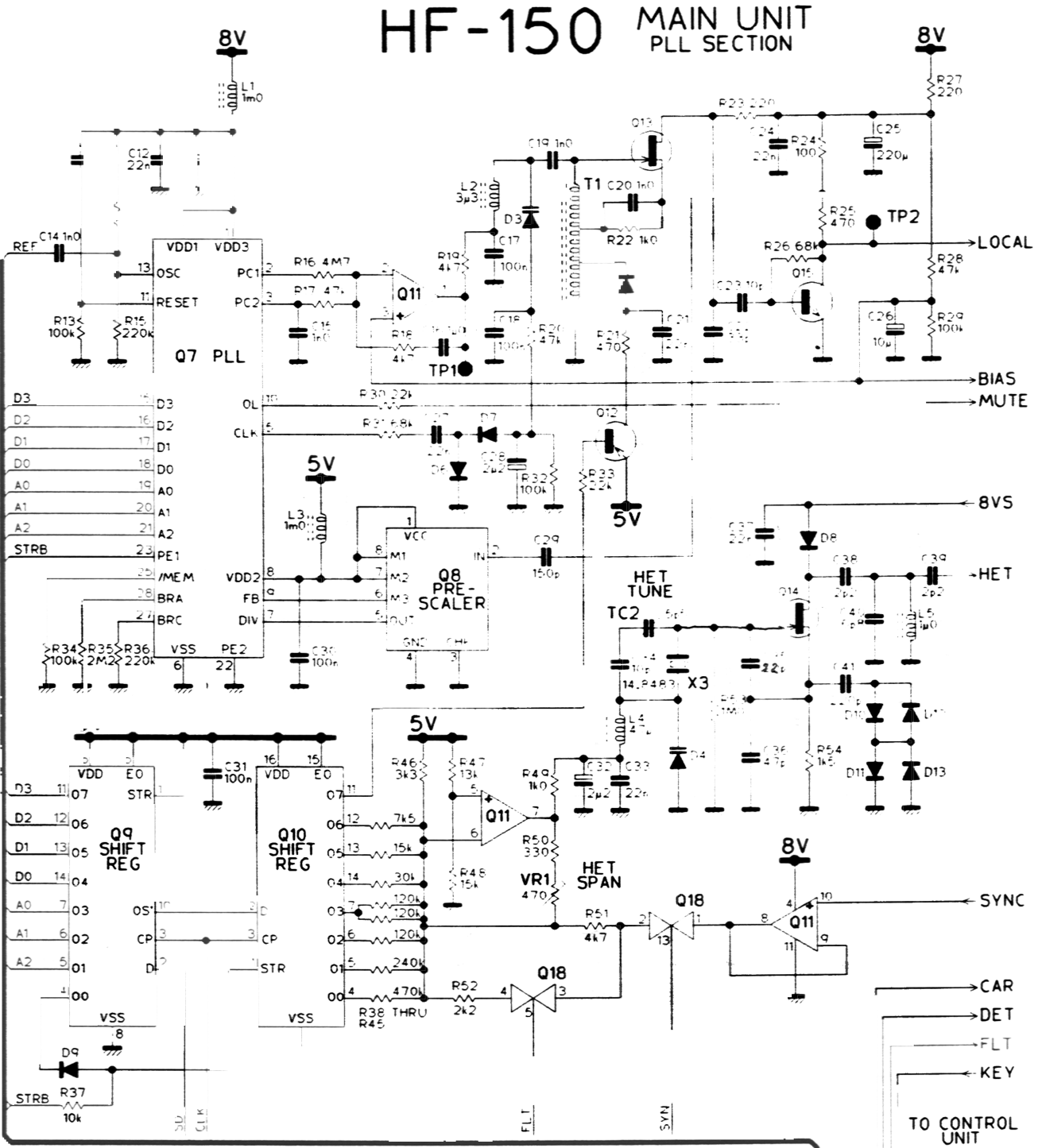


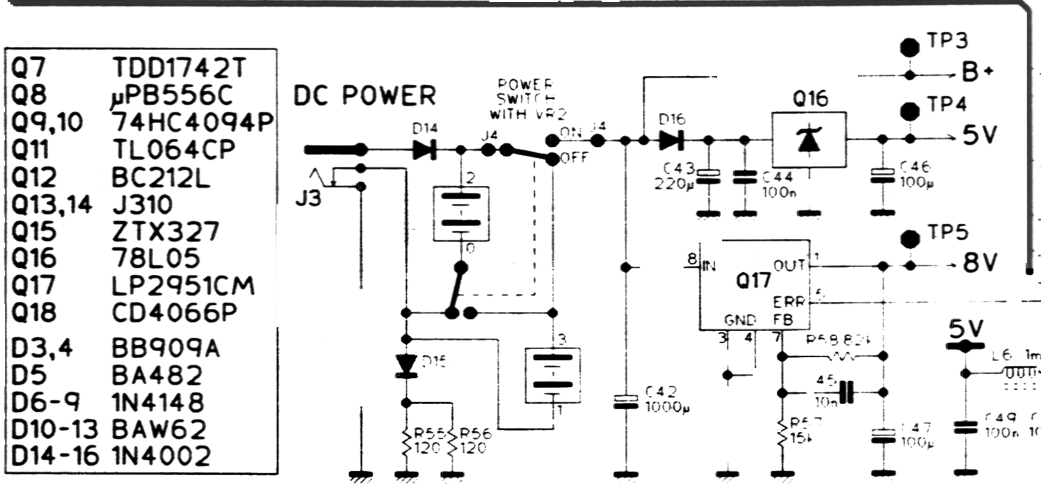
KPAD-1 EXTERNAL KEYPAD



IF-150 RS232 INTERFACE


HF-150 CONTROL UNIT
D1,2 1N4148
Q1 S83C751
Q2 ST93CS56B1
Q3 BC183L
Q4 MC14569BCP
Q5 74HC74P
Q6 MM5453N
BUTTONS
MEM
MODE
FAST
Q1 CPU
TUNING ENCODER
TO MAIN UNIT
REF ADJ
X2 7kHz
Q2 EEPROM
Q4 CAR GEN
Q5
Q6 DISPLAY DRIVER
SEGMENT OUTPUTS
LCD1
J1
J2
5VC

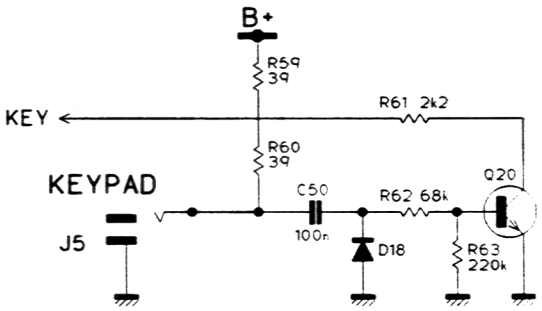


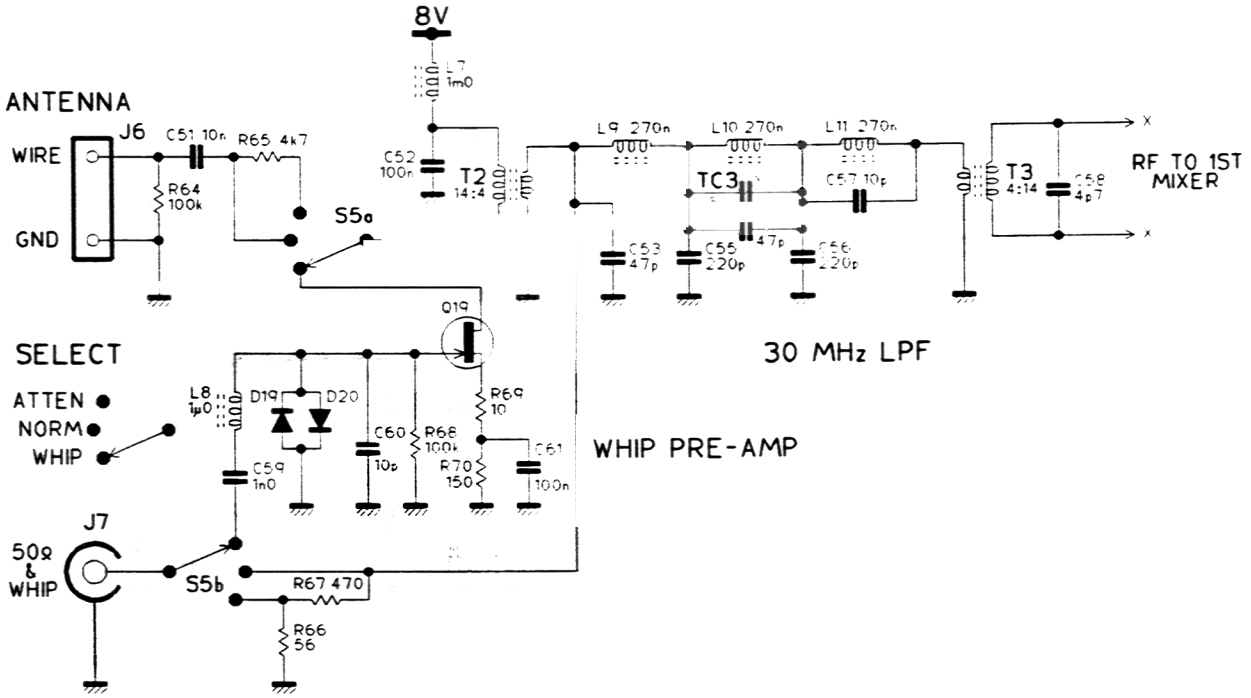


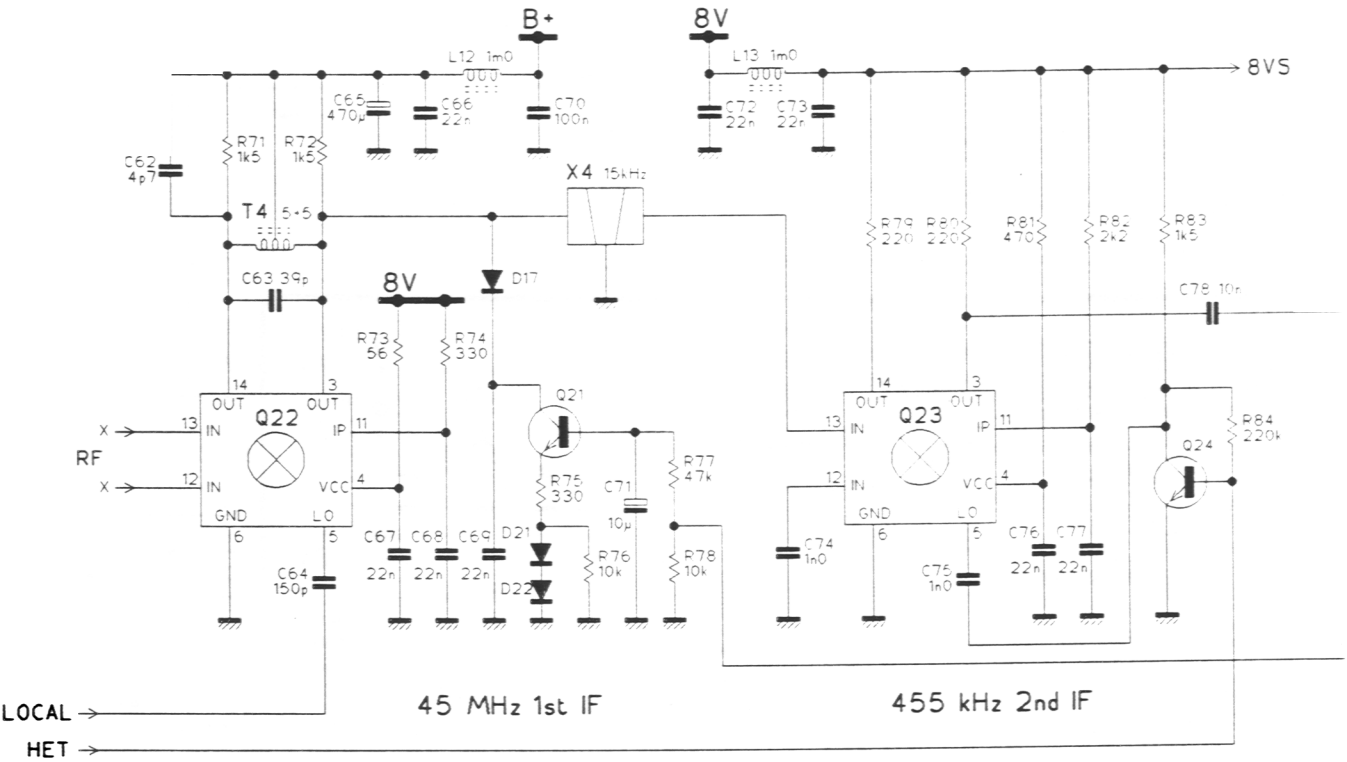
Q7	TDD1742T
Q8	µPB556C
Q9,10	74HC4094P
Q11	TL064CP
Q12	BC212L
Q13,14	J310
Q15	ZTX327
Q16	78L05
Q17	LP2951CM
Q18	CD4066P
D3,4	BB909A
D5	BA482
D6-9	1N4148
D10-13	BAW62
D14-16	1N4002

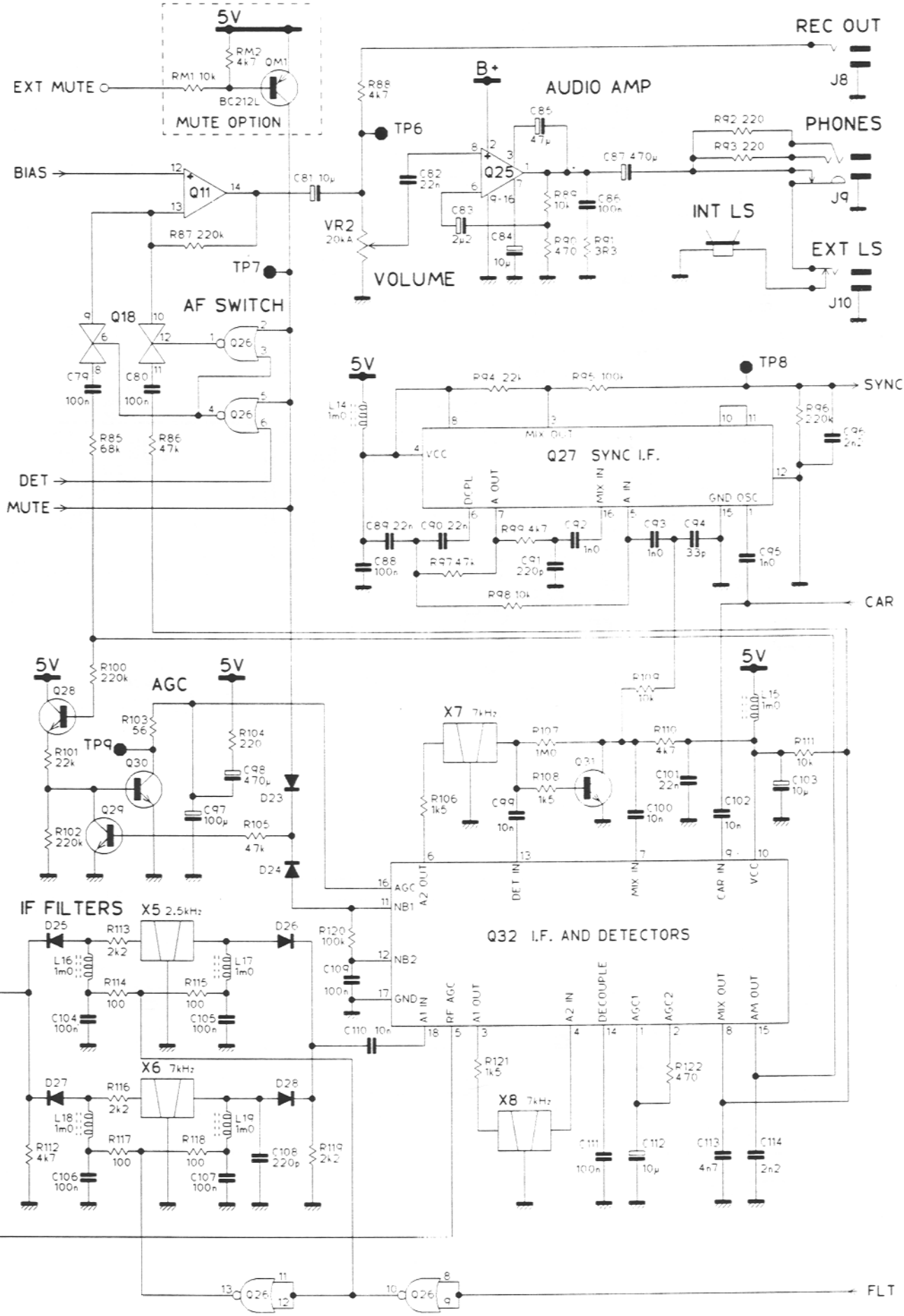
HF-150 MAIN UNIT RF and IF SECTION

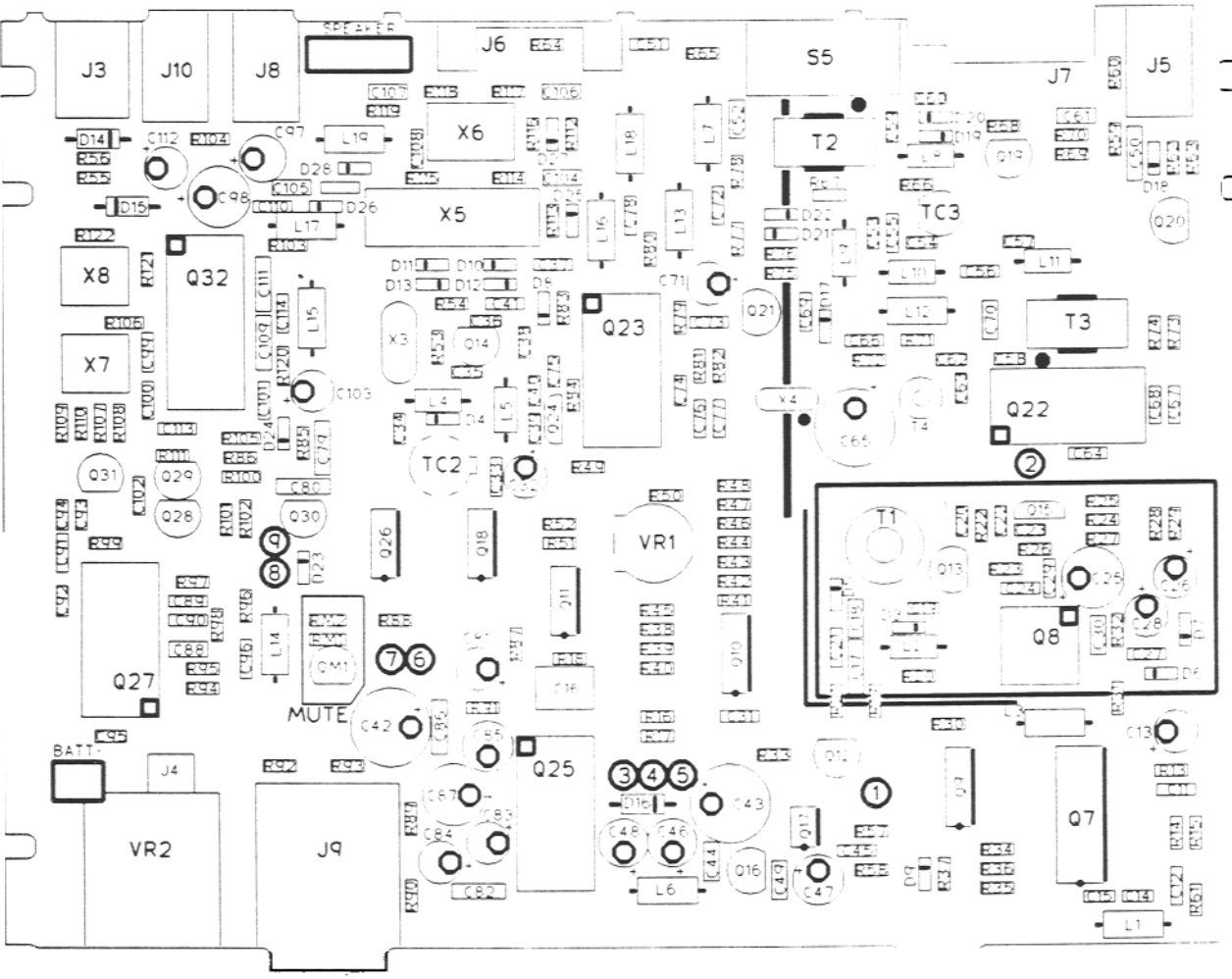
Q19	J310	Q27	MC3357P
Q20,21	BC183L	Q28-31	BC183L
Q22,23	SL6440CDP	Q32	SL6700CDP
Q24	ZTX320		
Q25	TDA1904	D17	MI204
Q26	74HC02	D18-28	1N4148

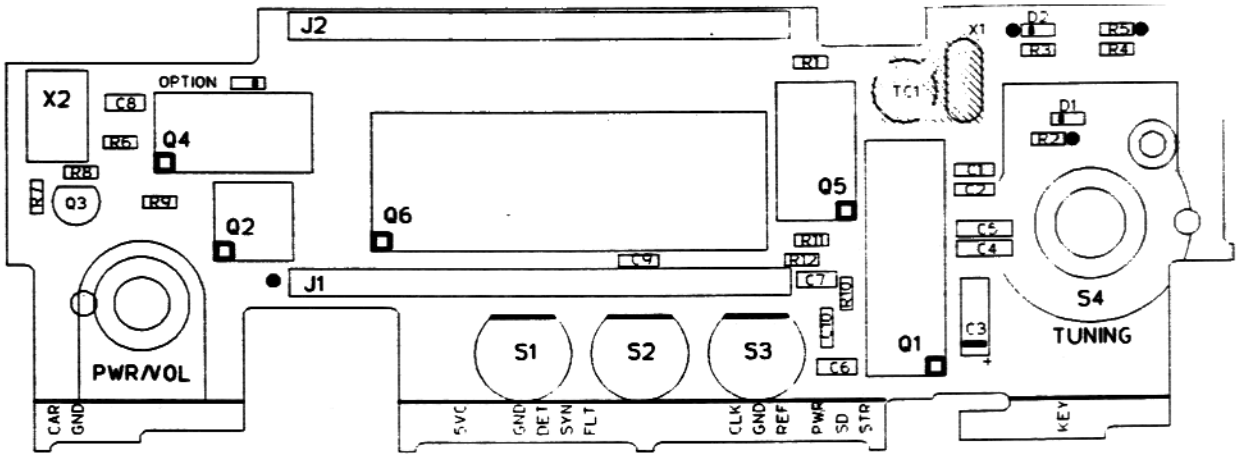







5V
RM2 4k7
QM1
RM1 10k
EXT MUTE
BC212L
MUTE OPTION
REC OUT
J8
B+
AUDIO AMP
R88 4k7
TP6
C85 47µ
R92 220
R93 220
PHONES
J9
BIAS
Q11
C81 10µ
C82 22n
Q25
C87 470µ
C83 2µ2
C84 10µ
R89 10k
C86 100n
R90 470
R91 3R3
INT LS
EXT LS
J10
VR2 20kA
VOLUME
R87 220k
TP7
AF SWITCH
Q18
Q26
C79 100n
C80 100n
R85 68k
R86 47k
DET
MUTE
TP8
SYNC
R94 22k
R95 100k
L14 1m0
Q27 SYNC I.F.
VCC
MIX OUT
DET OUT
A OUT
MIX IN
A IN
GND OSC
R96 220k
C96 2n2
C88 100n
C89 22n
C90 22n
R99 4k7
C92 1n0
C93 1n0
C94 33p
C95 1n0
R97 47k
C91 220p
R98 10k
CAR
R100 220k
Q28
AGC
R103 56
R104 220
TP9
Q30
Q29
R101 22k
R102 220k
C98 470µ
C97 100µ
R105 47k
D23
D24
R109 10k
X7 7kHz
R107 1M0
Q31
R108 1k5
R110 4k7
R111 10k
C101 22n
C103 10µ
R106 1k5
C99 10n
C100 10n
C102 10n
IF FILTERS
X5 2.5kHz
D25
D26
R113 2k2
L16 1m0
L17 1m0
R114 100
R115 100
C104 100n
C105 100n
R120 100k
C109 100n
C110 10n
Q32 I.F. AND DETECTORS
AGC
NB1
NB2
GND
A2 OUT
DET IN
MIX IN
CAR IN
VCC
RF AGC
A1 OUT
A2 IN
DECOUPLE
AGC1
AGC2
MIX OUT
AM OUT
A1 IN
R121 1k5
R122 470
X8 7kHz
C111 100n
C112 10µ
C113 4n7
C114 2n2
X6 7kHz
D27
D28
R116 2k2
L18 1m0
L19 1m0
R117 100
R118 100
R112 4k7
C106 100n
C107 100n
C108 220p
R119 2k2
FLT


J3
J10
J8
SPEAKER
J6
S5
J7
J5
X6
T2
TC3
X5
X8
Q32
Q23
T3
X7
Q22
TC2
T1
VR1
Q8
Q27
MUTE
Q25
Q7
BATT+
J4
VR2
J9


J2
X2
OPTION
Q4
Q3
Q2
Q6
Q5
J1
TC1
X1
D2
D1
S4
TUNING
PWR/VOL
S1
S2
S3
Q1
CAR
GND
5VC
GND
DET
SYN
FLT
CLK
GND
REF
PWR
SD
STR
KEY